Imperial Journal of Interdisciplinary Research (IJIR)
Vol-3, Issue-9, 2017
ISSN: 2454-1362, http://www.onlinejournal.in

Single-Phase Nine Level PWM Inverter with DC Source for Photovoltaic Systems

S. A. Priyadarshini[1], A. Durga Devi[2], R. Anbumozhi[3] &
G. Gabriel Santhosh Kumar[4]
[1,2,3,4]Assistant Professor, K.Ramakrishnan College of Engineering, Samayapuram, Trichy.

Abstract : *Nine-level inverters have tremendous applications in the power industry. They present a new set of features that are well suited for use in reactive power compensation. They typically synthesized voltage waveform reduces harmonic content. It may be easier to produce a high-power, high-voltage inverter with the multilevel structure and also voltage stresses are controlled. Increasing the number of voltage levels in the inverter without requiring higher ratings on individual devices can increase the power ratings. The unique feature of the multilevel inverters is to provide high switching frequencies with low switching losses. This paper gives an insight into PWM cascaded H-Bridge multilevel inverters. Detailed analysis of these inverters has been carried out and compared to know how the voltage stresses and switching losses reduced.*

Index Terms : *PWM, H-Bridge, multilevel inverter, Photovoltaic(PV) system, total harmonic distortion(THD).*

I.INTRODUCTION

Traditional power generation resources are decreasing fast and in addition causes greenhouse gases emission; however the demand for electric power is increasing. Therefore, renewable energy resources have attracted more and more attention over the last decades. Renewable power sources are difficult to be directly connected to the power grid due to their variable and intermittent nature [1]. Power-electronic converters technology plays an mportant role in integrating and utilizing these alternative energy sources into the electricity grid, and it is widely used and rapidly expanding as these applications become more integrated with the gridbased systems [2]. Multilevel converter topologies have drawn a large research interest over the last two decades due to their inherent merits compared with their conventional counterpart especially for medium or high-power applications.

The common characteristic of the SHE-PWM method is that the waveform analysis is performed using Fourier theory [13].The main challenge associated with SHE-PWM techniques isto obtain the analytical solution of the system of non-linear transcendental equations that contain trigonometric termswhich in turn provide multiple sets of solutions [14] and [15].A number of approaches have been proposed for attaining the solutions. These include optimization methods [14] and [15], genetic algorithms and Walsh functions,theory of resultants [11] and modulation based methods. The main objective of this paper is to present an efficient single-phase nine-level SHE-PWM inverter fed from a single dc-link source.

Therefore, the proposed technique resolves the issue of multiple independent dc-link sources requirement, where only one dclink source is used to generate a nine-level output voltage waveform, hence significantly reduces the size, the cost and the complexity of the inverter compared with the conventional counterpart. This makes the inverter very promising technology for renewable energy sources applications such as PV and fuel cell.

II. MULTILEVEL INVERTERS

Multilevel inverters have been attracting in favor of academia as well as industry in the recent decade for high-power and medium-voltage energy control. In addition, they can synthesize switched waveforms with lower levels of harmonic distortion than an equivalently rated two-level converter.The multilevel concept is used to decrease the harmonic distortion in the output waveform without decreasing the inverter power output. This paper presents the most important topologies like diode-clamped inverter (neutral-point clamped),capacitor-clamped (flying capacitor), and cascaded multilevel with separate dc sources.

The advantages of three-level Inverter topology over conventional two-level topology are:

- The voltage across the switches is only one half of the DC source voltage;
- The switching frequency can be reduced for the same switching losses;

• The higher output current harmonics are reduced by the same switching frequency.

Plentiful multilevel converter topologies have been proposed during the last two decades.

Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system for a high power application [1-3]. The concept of multilevel converters has been introduced since 1975 [4]. The term multilevel began with the three-level converter [5]. Subsequently, several multilevel converter topologies have been developed [6-13]. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources.

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel converter can be briefly summarized as follows.

- ***Staircase waveform quality*:** Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the *dv*/*dt* stresses; therefore electromagnetic compatibility (EMC) problems can be reduced.
- ***Common-mode (CM) voltage*:** Multilevel converters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced.
- ***Input current***: Multilevel converters can draw input current with low distortion.
- ***Switching frequency***: Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

2.1 Multilevel power converter structures

As previously mentioned, three different major multilevel converter structures have been applied in industrial applications: cascaded H-bridges converter with separate dc sources, diode clamped, and flying capacitors. Before continuing discussion in this topic, it should be noted that the term *multilevel converter* is utilized to refer to a power electronic circuit that could operate in an inverter or rectifier mode. The multilevel inverter structures are the focus of in this chapter; however, the illustrated structures can be implemented for rectifying operation as well.

2.2 Cascaded H-Bridges

A single-phase structure of an *m*-level cascaded inverter is illustrated in Figure2.1. Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+Vdc$, 0, and $-V$ by connecting the dc source to the ac output by different combinations of the four switches, *S* To obtain $+V$ switches *S2dc*, switches *S* and *S31* and *S*. By turning on *S4* are turned on, whereas $-V1$ and *S2* or *S3* and *S4dc dc1*, *S2*, *S3*, and *S*can be obtained by turning on , the output voltage is *0*. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels *m* in a cascade inverter is defined by $m = 2s+1$, where *s* is the number of separate dc sources. An example phase voltage waveform for an 11-level cascaded H-bridge inverter with 5 SDCSs and 5 full

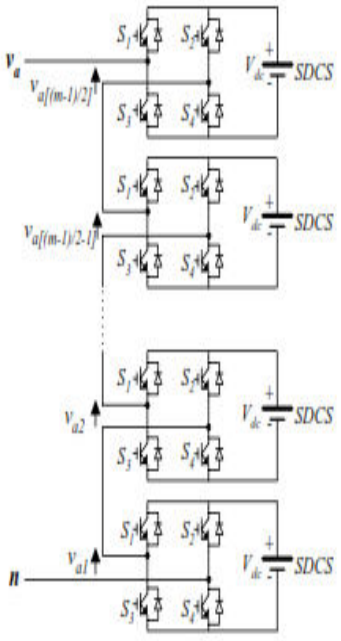


Fig 1 Single Level Structure Of A Multi Level Cascaded Bridge

2.3 Diode-Clamped Multilevel Inverter

The neutral point converter proposed by Nabae, Takahashi, and Akagi in 1981 was essentially a three-level diode-clamped inverter [5]. In the 1990s several researchers published articles that have reported experimental results for four-, five-, and six-level diode-clamped converters for such uses as static var compensation,

variable speed motor drives, and highvoltage system interconnections. A three-phase six-level diode-clamped inverter is shown in Figure2.2.Each of the three phases of the inverter shares a common dc bus, which has been subdivided by five capacitors into six levels. The voltage across each capacitor is *V* , and the voltage stress across each switching device is limited to *V* through the clamping diodes. Table 2.1 lists the output voltage levels possible for one phase of the inverter with the negative dc rail voltage *V 0dc* as a reference. State condition *1* means the switch is on, and *0* means the switch is off. Each phase has five complementary switch pairs such that turning on one of the switches of the pair requires that the other complementary switch be turned off. The complementary switch pairs for phase leg *a* are (*Sa1*, *Sa'1*), (*Sa2*, *Sa'2*), (*Sa3*, *S*), and(*Sa5*, *Sa'5a'3*). Table 2.1 also shows that in a diode-clamped inverter, the switches that are on for a particular phase leg are always adjacent and in eries. For a six-level inverter, a set of fiveswitches is on at any given time.), (*Sa4*, *Sa'4dc)*

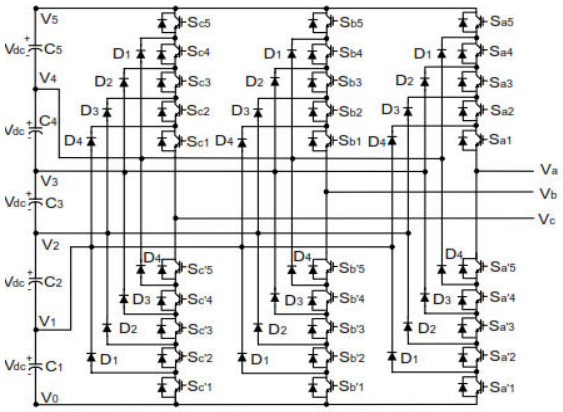


Fig 2 Three-Phase Six-Level Structure Of A Diode-Clamped Inverter**.**

Voltage V_{a0}	Switch State									
	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	$S_{a'5}$	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$V_5 = 5Vdc$	1	1	1	1	1	0	0	0	0	0
$V_4 = 4Vdc$	0	1	1	1	1	1	0	0	0	0
$V_3 = 3Vdc$	0	0	1	1	1	1	1	0	0	0
$V_2 = 2Vdc$	0	0	0	1	1	1	1	1	0	0
$V_1 = Vdc$	0	0	0	0	1	1	1	1	1	0
$V_0 = 0$	0	0	0	0	0	1	1	1	1	1

Table 1 diode-clamped six-level inverter voltage levels and corresponding switch states.

2.4 Three Level Inverter (TLI) Technology

This Application Note reviews three level inverter topology, often referred to as Neutral Point Clamped (NPC) inverter. The three level inverter offers several advantages over the more common two level inverter. As compared to two level inverters, three level inverters have smaller output voltage steps that mitigate motor issues due to long power cables between the inverter and the motor. These issues include surge voltages and rate of voltage rise at the motor terminals and motor shaft bearing currents. In addition, the cleaner output waveform provides an effective switching frequency twice that of the actual switching frequency. Should an output filter be required, the components will be smaller and less costly than for an equivalent rated two level inverter. Most often the NPC inverter is used for higher voltage inverters. Because the IGBTs are only subjected to half of the bus voltage, lower voltage IGBT modules can be used.

2.4.1Basic Circuit Configuration and Its Behavior

Figure 1 shows the circuit configuration of the NPC inverter. Each leg has four IGBTs connected in series.The applied voltage on the IGBT is one-half that of the conventional two level inverter. The bus voltage is split in two by the connection of equal series connected bus capacitors. Each leg is completed by the addition of two clamp diodes.

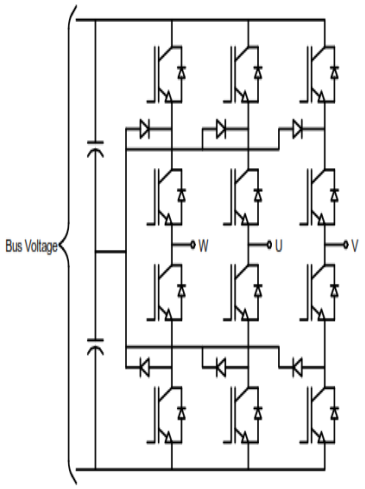


FIG 3 NPC Inverter

2.4.2 Ouptut Voltage and Switching States

The NPC inverter can produce three voltage levels on the output: the DC bus plus voltage, zero voltage and DC bus negative voltage. The two level inverter can only connect the output to either the plus bus or the negative bus. (Refer to Figure 2.3 for the following example.) For a one

phase operation, when IGBTs Q1 and Q2 are turned on, the output is connected to Vp; when Q2 and Q3 are on, the output is connected to V0; and when Q3 and Q4 are on, the output is connected to Vn.

Switching states for the four IGBTs are listed in Table 1. Clamp diodes D4 and D5 provide the connection to the neutral point. From the switching states, it can be deduced that IGBTs Q2 and Q3 are on for most of the cycle, resulting in greater conduction loss than Q1 and Q4 but far less switching loss. In addition, the free wheel diodes for Q2 and Q3 are for most cases, soft switched as the IGBT parallel to the diode is on, thus holding the recovery voltage across the diode to that of the IGBT Vce.

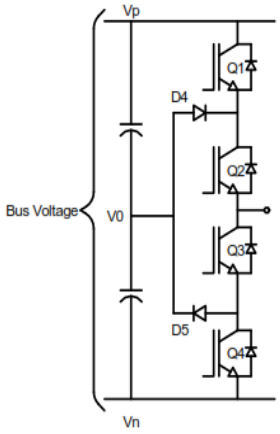


Fig 4 Single Leg

IGBT	Vout = Vp	Vout = V0	Vout = Vn
Q1	On	Off	Off
Q2	On	On	Off
Q3	Off	On	On
Q4	Off	Off	On

TABLE 2 Switching States

III. PROPSED SYSTEM AND SIMULATION RESULTS

The photovoltaic cell output voltage is basically a function of the photocurrent which is mainly determined by load current depending on the solar irradiation level during the operation.

$$V_C = (A*K*T_C/e)\ln((I_{ph}+I_o-I_c)/I_o)-R_S*I_C$$

The symbols used are

Vc : cell output voltage, V.

Tc : reference cell operating temperature (20 °C).

Rs: series resistance of cell (0.001 O).

Iph: photocurrent, function of irradiation level and junction temperature (5 A).

I0: reverse saturation current of the diode (2*10-4 A).

Ic: cell output current, A.

k: Boltzmann constant (1.38 × 10-23 J/K).

e: electron charge (1.602 × 10^-19 C).

For accurate modeling of the solar panel, two diode circuit could have been used. But our scope of study is limited to single diode model. Following are the ideal characteristics of a solar array which show the variation of current and voltage with respect to voltage.

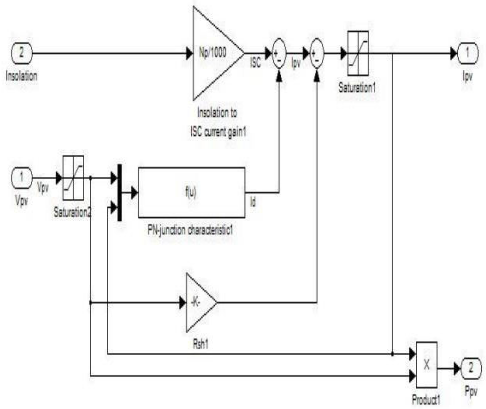


Fig 5 Simulink model of PV

4.5 Algorithms

The three main versions of the hill climbing algorithm are P&O, MP&O and EPP.P&O has been described below.

Perturb and Observe

In this algorithm a slight perturbation is introduced in the system. Due to this perturbation, the power of the module alters. If the power enhances due to the perturbation, then the perturbation is carried on in that direction. After the maximum power is accomplished, the power at the next instant decrements and hence the perturbation reverses.Among different maximum power point tracking algorithms, the perturb and observe algorithm is elementary and also gives desirable results. This algorithm is chosen and certain changes are made in the current work. The flow chart of the method is shown in the fig 20. The algorithm takes the values of current and voltage from the solar photovoltaic module. Power is computed from the assessed voltage and current. The values of voltage and power at k Then next values at (k+1)thth instant are put in. instant are measured again and power is calculated from the measured values. The power and voltage at (k+1)th

instant are subtracted with the values from previous instant. If we detect the power voltage curve of the solar photovoltaic module we see that in the right hand side curve where the voltage is almost constant the slope of power voltage is negative (dP/dV<0) where as in the left hand side the slope is positive and dP/dV>0. The right side curve is for the lower duty cycle (nearer to zero) whereas the left side curve is for the higher duty cycle (nearer to unity). Depending on the sign of dP(P(k+1) - P(k)) and dV(V(k+1) -V(k)) after subtraction the algorithm decide whether to increase the duty cycle or to reduce the duty cycle. The algorithm is elementary and has only one loop [11].

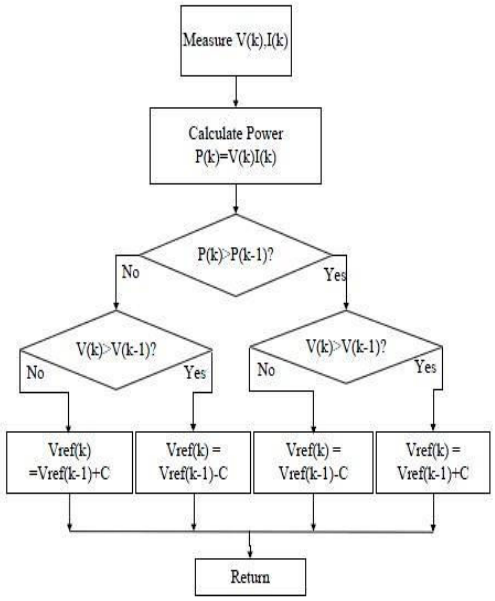


Fig 6 Flowchart Of P&O Algorithm

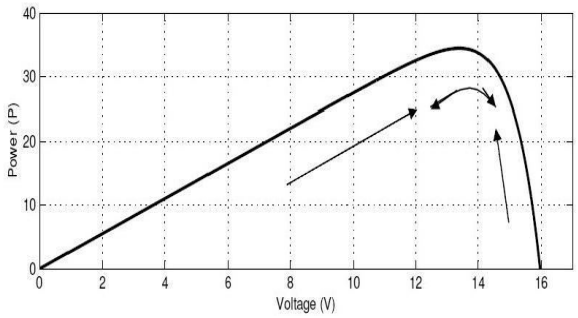


Fig 7 Perturb And Observe Algorithm

A novel PWM modulation technique was introduced to generate the PWM switching signals. Three reference signals (*V*ref1, *V*ref2, and *V*) were compared with a carrier signal (*Vcarrier*ref3). The reference signals had the same frequency and amplitude and were in phase with an offset value that was equivalent to the amplitude of the carrier signal. The reference signals were each compared with the carrier signal. If *V* had exceeded the peak amplitude of *V*carrier, *V*ref2ref1 was compared with *V* until it had exceeded the peak amplitude of *V* carrier carrier . Then, onward, *V* would take charge and would be compared with *V* until it reached zero. Once *V* ref3 had reached zero, *V*ref3 carrier would be compared until it reached zero. Then, onward, *V*ref2 would be compared with *V*carrierref1

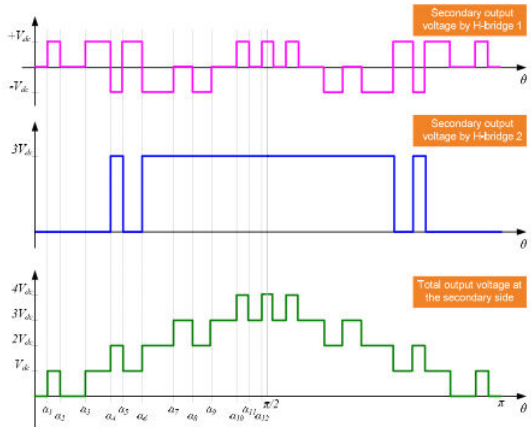


Fig 8 Switching pattern for single phase nine level inverter

Mode 1 : $0 < \omega t < \theta 1$ and $\theta 4 < \omega t < p$

Mode 2 : $\theta 1 < \omega t < \theta 2$ and $\theta 3 < \omega t < \theta 4$

Mode 3 : $\theta 2 < \omega t < \theta 3$

Mode 4 : $p < \omega t < \theta 5$ and $\theta 8 < \omega t < 2p$

Mode 5 : $\theta 5 < \omega t < \theta 6$ and $\theta 7 < \omega t < \theta 8$

Mode 6 : $\theta 6 < \omega t < \theta 7$.

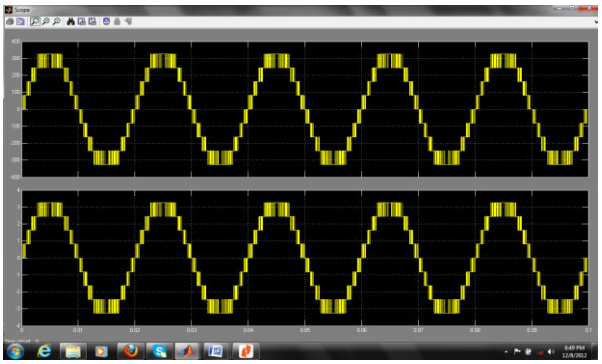
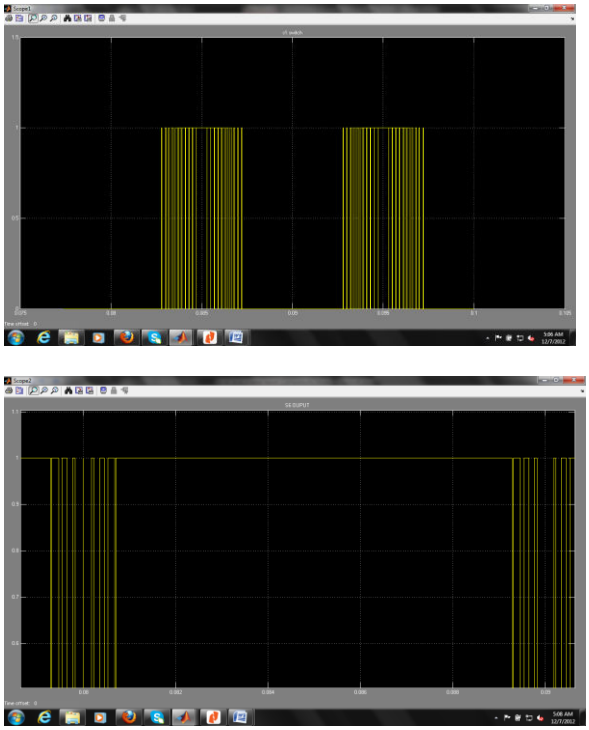


Fig 10 Output of nine level inverer

Fig 11 Output of the switches



IV CONCLUSION

Multilevel inverters offer improved output waveforms and lower THD. This paper has presented a novel PWM switching scheme for the proposed multilevel inverter. It utilizes three ref-erence signals and a triangular carrier signal to generate PWM switching signals. The behavior of the proposed multilevel inverter was analyzed in detail. By controlling the modulation index, the desired number of levels of the inverter's output voltage can be achieved.The less THD in the nine-level inverter is an attractive solution for photovoltaic systems.

References

[1] M. Calais and V. G. Agelidis, "Multilevel converters for single-phase grid connected photovoltaic systems—An overview," in *Proc. IEEE Int. Symp. Ind. Electron.*, 1998, vol. 1, pp. 224–229.

[2] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.

[3] P. K. Hinga, T. Ohnishi, and T. Suzuki, "A new PWM inverter for photovoltaic power generation system," in *Conf. Rec. IEEE Power Electron.Spec. Conf.*, 1994, pp. 391–395.

[4] Y. Cheng, C. Qian, M. L. Crow, S. Pekarek, and S. Atcitty, "A comparison of diode-clamped and cascaded multilevel converters for a STATCOM with energy storage," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1512–1521, Oct. 2006.

[5] M. Saeedifard, R. Iravani, and J. Pou, "A space vector modulation strategy for a back-to-back five-level HVDC converter system," *IEEE Trans. Ind.Electron.*, vol. 56, no. 2, pp. 452–466, Feb. 2009.

[6] S. Alepuz, S. Busquets-Monge, J. Bordonau, J. A. M. Velasco, C. A. Silva, J. Pontt, and J. Rodríguez, "Control strategies based on symmetrical components for grid-connected converters under voltage dips," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2162–2173,Jun. 2009.

[7] J. Rodríguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[8] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[9] M. M. Renge and H. M. Suryawanshi, "Five-level diode clamped inverter to eliminate common mode voltage and reduce dv/dt in medium voltage rating induction motor drives," *IEEE Trans. Power Electron.*, vol. 23,no. 4, pp. 1598–1160, Jul. 2008.

[10] E. Ozdemir, S. Ozdemir, and L. M. Tolbert, "Fundamental-frequencymodulated six-level diode-clamped multilevel inverter for three-phase stand-alone photovoltaic system," *IEEE Trans. Ind. Electron.*, vol. 56,no. 11, pp. 4407–4415, Nov. 2009.

[11] R. Stala, S. Pirog, M. Baszynski, A. Mondzik, A. Penczek, J. Czekonski, and S. Gasiorek, "Results of investigation of multicell converters with balancing circuit—Part I," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7,pp. 2610–2619, Jul. 2009.

[12] R. Stala, S. Pirog, M. Baszynski, A. Mondzik, A. Penczek, J. Czekonski, and S. Gasiorek, "Results of investigation of multicell converters with balancing circuit—Part II," *IEEE Trans. Ind.*

Electron., vol. 56, no. 7,pp. 2620–2628, Jul. 2009.

[13] P. Lezana, R. Aguilera, and D. E. Quevedo, "Model predictive control of an asymmetric flying capacitor converter," *IEEE Trans. Ind. Electron.*,vol. 56, no. 6, pp. 1839–1846, Jun. 2009.

[14] M. F. Escalante, J.-C. Vannier, and A. Arzandé, "Flying capacitor multilevel inverters and DTC motor drive applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 809–815, Aug. 2002.

[15] A. Shukla, A. Ghosh, and A. Joshi, "Static shunt and series compensations of an SMIB system using flying capacitor multilevel inverter," *IEEE Trans. Power Del.*, vol. 20, no. 4, pp. 2613–2622,Oct. 2005.