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# Design and Parametric Analysis of Dual Work Function Pile Gate Approach for Low Leakage FinFET

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***Abstract:*** *According to Moore's law scaling of CMOS technologies beyond 22nm is limited by factors like excessive power consumption, process variation effects and other short channel effects (SCEs) like Drain Induce Barrier Lowering (DIBL), Gate Induce Drain Leakage (GIDL) and $V_{th}$ roll off. Double Gate MOSFETs (DG MOSFET) is one of the solution to these SCEs but due to fabrication difficulties like misalignment of top and bottom gates etc. DG MOSFETs are replaced by FinFET. FinFET (Fin Field-Effect Transistor) innovation has as if now observed a noticeable increment in the selection of inbuilt circuits due to its high sensitivity to short channel impacts and its further strength to scale it down. Already, a noticeable research work was made to reduce the leakage current in the standard bulk devices. Such a large number of various choices like mass separation and oxide confinement are all having a few pros and cons. Here in this work, a novel Pile gate FinFET structure is introduced to overcome the short channel effects, unlike from Bulk FinFET without utilizing any pstop implant or isolation oxide as in the Silicon-on-Insulator (SOI). The real favorable position of this kind of structure is that there is no need of high substrate doping, a 100% decrement in the random dopant fluctuation (RDF) and an expansion in the $I_{ON}/I_{OFF}$ esteem. It can be exceptionally valuable to enhance the drain-induced barrier lowering (DIBL) at smaller tech. For the simulation of modelled and designed structure Cogenda Visual TCAD 1.8.0.4 tool has been used.*

*Keywords*: Short channel effects, Pile Gate FinFET, Leakage current, Bulk MOSFET

## 1. Introduction

The journey of the modern MOSFETs has been started in 1959 when Dawon Kahng and Martin M. John invented the MOSFET at Bell Labs. Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a four terminal device i.e. source(S), gate (G), drain (D) and body (B). It is used for amplifying or switching the electronic signals. MOSFET can be differentiated into two types as n channel MOSFET in which channel contains electrons and p channel MOSFET containing holes in channel. MOSFET have two modes enhancement mode in which the conductivity increases by increasing the carriers in the channel and depletion mode in which conductivity decreases by decreasing carriers in channel when the gate voltage is applied.

For several decades, as predicted by Moore' Law the semiconductor industry witnesses that the number of transistors per integrated circuits is increasing exponentially. Due to relentless progress in silicon-based CMOS technology, there is hugely evolution of electronics, IT, and communications. Dimensional scaling is the main reason for this continuous progress. CMOS scaling technology is the main driving force for the improvement in device density and performance. With every new technology generation, the cost per function is reducing which increases economic efficiency.

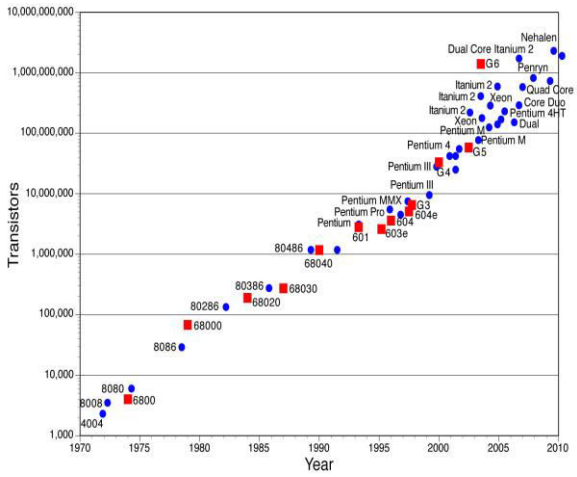


Fig 1: Moore's Law

When CMOS technology scaling enters the sub-micron region, various serious problems come into play like short channel effects (SCEs) or the small geometry effects. Some of these effects are such as a difficulty in increasing on current, increase leakage currents, the discrepancy in parameter, low yield and reliability and manufacturing cost increases etc. With a specific end goal to lessen the short channel effects in bulk MOSFET and SOI MOSFETs, DGMOSFET has been introduced. In spite of the fact that DGMOSFET suppresses many of the short channel effects, the trouble in the fabrication of DGMOSFET has been encountered because of the misalignment of top gate and the back gate. Hence to defeat the shortcomings of DGMOSFET the FinFET design is introduced.

In the FinFET the conducting channel is raised up into a "fin" with the gate wrapped around it in a 3dimensional structure as shown in Figure 3.1, Hfin is the tallness of fin, Lg is the gate length and Wfin is the width of the fin. The fundamental advantage of a FinFET is that no part of the channel is not too a long way from the influence of the gate hence the controllability of gate over channel increases and the gadget can be turn on-off rapidly.

## 2 Silicon on Insulators MOSFET's (SOI MOSFET)

CMOS integrated circuits are solely created on bulk silicon substrates for two clear reasons: the abundant supply of silicon wafers, and in light of the fact that the great oxide can be promptly grown on silicon, which is not possible on germanium or on some different semiconductors. The primary motivation for scaling CMOS gadgets is the increased functionality per cost and the improved performance of gadgets. Scaling requires these thin entryway insulators keeping in mind the end goal to have low short channel effects and to increase performance, however, tunneling spillage current flowing through these thin insulators is one of the disadvantages for many applications. Shallow trench isolation (STI) is utilized to separate the FETs, which brought about high circuit density.

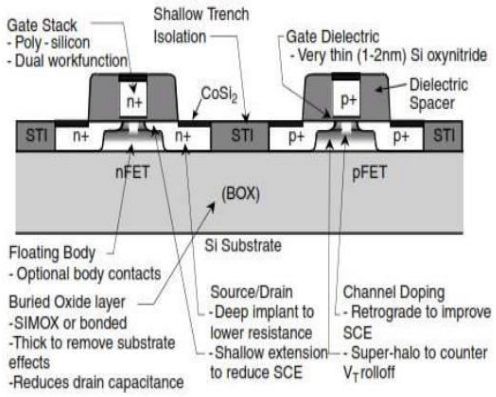


Figure 2: PD-SOI MOSFET

In a request to prevent degradation of the insulator of the entryway because of hot electrons and to lessen short channel effects, the combination of deep and shallow implants are to be perfectly engineered which is utilized for the source and drain. SOI MOSFET can be characterized into two parts given as:

### a) Partially Depleted (PD) SOI MOSFET:

In this type of MOSFET, the silicon film thickness is larger than the sum of the width of depletion region from back to front end. Hence there is no interaction between source/drain and buried oxide due to which a neutral piece remains beneath the depletion region

In the event that this piece will connect to the ground or body contact, it will act as a bulk MOSFET. In the event that this piece remains neutral or not connected to any contact than it winds up noticeably floating giving ascent to Kink effect or floating body effect, degrading the qualities of the gadget. In PD-SOI MOSFET, the depletion region is thinner as compared to the silicon layer because of which some undepleted silicon goes about as the floating body for the gadget. The buried oxide (BOX) layer insulates the gadget layer from the substrate. This construction brings about a source and drain-to-body junction capacitances that are significantly diminished, which can increase digital switching speed. Because of floating body effect, the dependencies of bulk MOSFET body effect on the source to substrate voltage eliminates.

### b) Fully Depleted (FD) SOI MOSFET:

In this structure, the silicon layer is thinner as compared to PD-SOI MOSFET. With a specific end goal to remain completely depleted and full control on short channel effects, the layer should benefit from the depletion depth of bulk MOSFET. The elimination of floating body effect, simple circuit design and drain capacitance reduction are a portion

of the advantages of FD-SOI MOSFET over PD-SOI MOSFET.

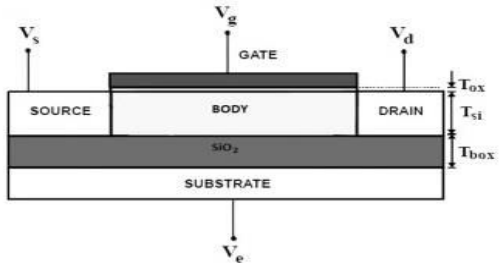


Figure 3: FD- SOI MOSFET

It is hard to control the thickness of thin silicon layer which prompts trouble in controlling the limit voltage (depends on the silicon thickness) and trouble in achieving low resistance at a source and drain contacts for thin silicon layer for the situation of FD-SOI MOSFET. The last problem can be measured by raising the source/drain process. There is another problem related with PD-SOI MOSFET is that self-heating of the gadget because of the lower warm conductivity of silicon oxide. Because of generation of warmth in the drain of MOSFET, this causes heating of the gadget because of which the mobility diminishes.

## 3 Multi-gate MOSFET and FINFET

Another method for eliminating deeply submerged leakage paths is to provide door control from more than one side of the channel as shown in Fig. The silicon film is thin so that no leakage path is a long way from one of the entryways. (The most pessimistic scenario path is along the center of the silicon film.) Therefore, the gate(s) can suppress leakage current more effectively than the conventional MOSFET. Since there are more than one doors, the structure might be called multi-entryway MOSFET. The structure shown beneath might be called as Double Gate MOSFET.

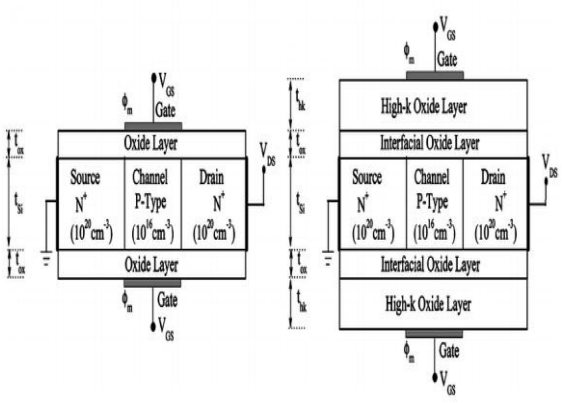


Figure 4: Cross sectional view of DG- MOSFET

[3] Kaushik Roy, Saibal *Mukhopadhya* and Hamid Mahmoodi, "Leakage Current Mechanisms and Leakage reduction techniques in deep sub-micron CMOS Circuits", *Proc. of IEEE, vol.91, no.2, pp.305-327, February 2003.*; describes that the nonstop scaling of channel length, gate oxide thickness, and the limit voltage in the deep-sub micrometer administration prompts high leakage current which is turning into a genuine concern in perspective of the powerful dissipation. Along these lines, it is important to distinguish distinctive leakage segments and to precisely indicate them so as to diminish the leakage power. This paper reviews the various transistor inborn leakage frameworks, including sub-limit leakage, deplete instigated obstruction bringing down, punch through, gate prompted deplete leakage, hot carrier infusion into the oxide, and entryway oxide burrowing. The paper in like manner examines channel building methodologies including radiance doping and retrograde doping as an approach to improve short-channel impacts for consistent scaling down of CMOS devices. At long last, the paper reveals different systems to diminish leakage power. The technological challenges in realizing this new gadget structure are likewise presented in this paper. Double Gate MOSFETs provide excellent short channel effect immunity and display a near perfect sub-edge slope which makes them a definitive adaptable gadget structure.

## 4 Dual work function Pile Gate Structure

This paper describes about the novel dual work function Pile gate FinFET structure to overcome the short channel effects, unlike from Bulk FinFET without utilizing any pstop implant or isolation oxide as in the Silicon-on-Insulator (SOI).

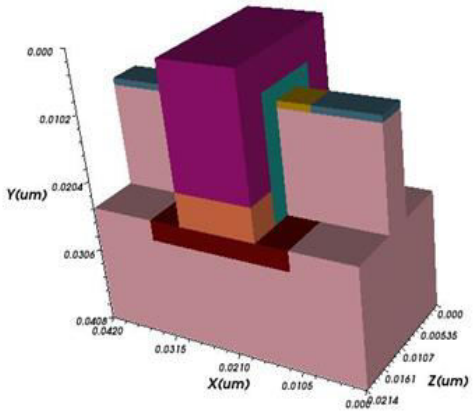


Figure 5: Dual work function Pile Gate FinFET

## 5 Result and Discussion

The Pile gate FinFET with a channel length of 12 nm, fin width of 5 nm, power supply of 0.75V at saturation region and 0.05V at the linear region is utilized. Proposed pile-gate gadgets are simulated and optimized for different parameters, for example, channel doping, the stature of bottom gate, the number of fins, and so forth. To obtain characteristics of conventional Bulk FinFET structure, we applied constant drain voltage ($V_{DS}$), and provide variation in gate voltage ($V_{GS}$). Figure 6 show the drain characteristics of pile gate FinFET.

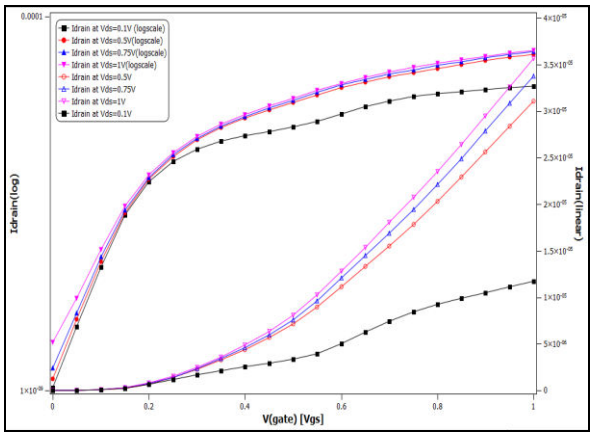


Figure 6: Drain current versus Gate voltage curve for Pile gate FinFET at different drain voltages in log and linear scale

Figure 7 shows the drain characteristics with the variation in work function of bottom gate in Pile gate FinFET. The higher the gate work function, lower the OFF current. But while choosing the work function, we have to maintain the highest $I_{ON}/I_{OFF}$. So trade-off can be made between leakage current and on-off current ratio.

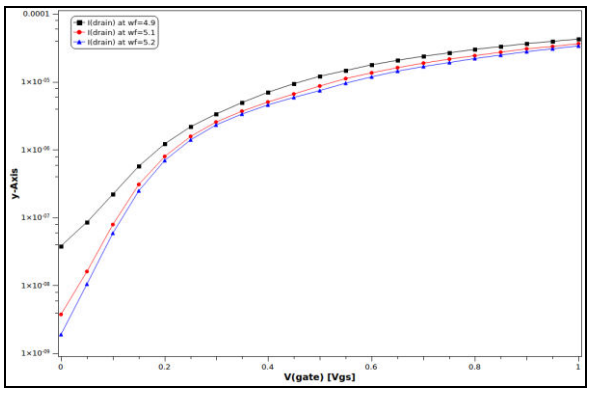


Figure 7: Drain characteristics for Pile gate FinFET with variation in work function of bottom gate

Table 1 shows the off state current values with the variation in work function of bottom gate.

Table 1: Off state current at different gate work function

| Work function | Ioff |
|---|---|
| 4.9eV | 38nA |
| 5.1eV | 3.8nA |
| 5.2eV | 1.9nA |

## Conclusion

It is watched that by incorporating the bottom gate with the high work-function, the Pile gate FinFET can accomplish less leakage current compared to the Bulk FinFET and still have an improved ION/IOFF. With the help of dual work function Pile gate structure, it can be seen that $I_{OFF}$ is less if there should arise an occurrence of pile gate FinFET which brings about the higher estimation of $I_{ON}/I_{OFF}$ esteems. This happens on the grounds that in thin this structure, the bottom gate work function is especially higher than the top gate, so for the applied gate bias, the bottom part of the fin near the fin substrate interface appears to remain in the accumulation, causing leakage and additionally because of the higher work-function bottom gate, the surface potential of the zone near the channel and substrate increases. Along these lines, the potential hindrance for the electrons causes the leakage under the channel, so higher obstruction tallness electrons find it hard to move from source to drain and subsequently it helps in suppressing drain-induced boundary lowering (DIBL).

## References

[1] G.Moore, “Cramming more components into integrated circuits”, *Proc. of IEEE, vol. 86, no. 1, January 1998.*

[2] J.R.Brews, W. Finchtner, E.H. Nicollian, S.M. Sze, "Generalized Guide for MOSFET Miniaturization" , *Proc. of IEEE ,vol.2, pp.10-13, 1979.*

[3] Kaushik Roy, Saibal Mukhopadhya and Hamid Mahmoodi, "Leakage Current Mechanisms and Leakage reduction techniques in deep sub-micron CMOS Circuits", *Proc. of IEEE, vol.91, no.2, pp.305-327, February 2003.*

[4] Vishwas Jaju, "Silicon on Insulator Technology", *spring 2004.*

[5] Ran-Hong Yan, Abbas Ourmazd and Kwing F.Lee, "Scaling the Si MOSFET: From Bulk to SOI to Bulk”, IEEE *Transactions on Electron Devices, vol.39, no.7, July 1992.*

[6] Kunihiro Suzuki, Testu Tanaka, Yoshiharu, Hiroshi Horie and Yoshihiro, "Scaling Theory for Double-Gate SOI MOSFET's" ,*IEEE Transactions On Electronic Devices, vol.40, no.12, December 1993.*

[7] Yaun Taur, "Analytic Solutions of Charge and Capacitance in Symmetric and Assymetric Double-Gate MOSFETs", *IEEE Transactions on Electron Devices, vol.48, no.12, December 2001.*

[8] Yaun Taur, Xiaoping Liang, Wei Wang and Huaxin Lu, " A Continuous, Analytic Drain - Current Model for DG MOSFETs" ,*IEEE Electron Device Letters, vol.25, no.2, February 2004.*

[10] Jin He, Xuemei Xi, Mansun Chan, Chung-Hsun Lin, Ali Niknejad and Chenming Hu, " A Non-Charge-Sheet Based Analytical Model of Undoped Symmetric Double gate MOSFETs using SPP Approach" ,*IEEE Conference, 2004.*

[11] Marc Swinnen and Ron Duncan, "Physical Verification of FinFETs and Fully Depleted SOI" *White paper synopsis, 2012*

[12] D.Jackuline Moni, R.Matarkodi, B.Suresh, "Device Level Analysis of Threshold Voltage Variation in FinFET with Varied design Parameters", *ICCCET, March 2011.*

[13] Digh Hisamoto, Wen-Chen Lee, Jakub Kedzierski, Hideki Takeuchi, Kazuya Asano, Charles kuo, Erik Anderson, Tsu-Jae King, Jeffrey Bokor and Chenming Hu, "FinFET- A Self Aligned Double-Gate MOSFET Scalable to 20nm" ,*IEEE Transactions on Electron Devices, vol.47, no.12, December 2000.*

[14] Daniel Pham, Larry Larson and Ji-Woon Yang, "FINFET Device Junction Formation Challenges", *IEEE Conference, 2006.*

[15] A.Kaneko, A.Yagishita, K.Yahashi, T.Kubota, M.Omura, K.Matsuo, I.Mizushima, K.Okano, H. Kawasaki, S.Inaba, T.Izumida, T.Kanemura, N.Aoki, K.Ishimaru, H.Ishiuchi, K.Suguri, K.Eguchi, Y.Tsunashima, "Sidewall Transfer Process and Selective Gate Sidewall Spacer Formation Technology for Sub-15nm FinFET with Elevated Source/Drain Extension" ,*IEEE Conference , 2005.*

[16] A.Dixit, K.G. Anil, R.Rooyackers, F.Leys, M.Kaiser, N.Collaert, K.De Meyer, M. Jurczak, S.Biesemans, "Minimization of specific contact resistance in multiple gate NFETs by selective epitaxial graowth of Si in HDD regions", *Solid State Electron, vol.50, pp. 587-593, 2006.*

[17] Yongxun Liu, Kenichi Ishii, Toshiyuki Tsutsumi, Meishoku Masahara and Eiichi Suzuki, "Ideal Rectangular Cross-Section Si-Fin Channel Double-Gate MOSFETs Fabricated Using Orientation-Dependent Wet Etching", *IEEE Electron Device Letters, vol.24, no.7, July 2003.*

[18] F.Dauge, J.Pretet, S.Cristoloveanu, A.Vandooren, L.Mathew, J.Jomaah, B.-Y Nguyen, "Coupling effects and channel seperation in FinFETs", *Solid State Electron, vol.48, pp.535-542, 2004.*

[19] Yaun Taur, Jooyoung Song, Bo Yu, "Compact Modelling of Multiple Gate MOSFETs", *IEEE Conference, 2008.*

[21] Alexander Kloes, Michaela Weidemann, Mike Schwarz, "Analysis of 3D Current Flow in Undoped FinFET and Approaches for Compact Modelling", *International Conference MIXDES, July 2009.*

[22] Alexander Kloes, Michaela Weidemann, Mike Schwarz, "Analytical current equation for short channel SOI Multigate FETs including 3D effects", *Solid State Electron, vol.54, pp.1408-1415, 2010.*

[23] Nikolaos Fasarakis, Andreas Tsormpatzoglou, Dimitrious H.Tassis, Illias Pappas, Konstantinos Papathanasiou, Matthias Bucher, Gerard Ghibaudo, Charalabos A. Dimitriadis, "Compact Model of Drain Current in Short-Channel Triple Gate FinFETs", *IEEE Transactions on Electron Devices ,vol. 59, no.7,pp.1891-1897, July 2012.*

[24] K.Papathanasiou, C.G. Theodorou, A.Tsormpatzoglou, D.H. Tasis, C.A. Dimitriadis, M.Bucher, G.Ghibaudo, "Symmetrical unified compact model of short-channel double-gate MOSFETs", *Solid State Electron, vol.69, pp.55-61, 2012.*

[25] Huaxin Lu, Bo Yu, Yaun Taur, "A unified charge model for symmetric double gate and surrounding-gate MOSFETs", *Solid State Electron, vol.52, pp.67-72, 2008.*

[26] N.Fasarakis, A.Tsormpatzoglou, D.H. Tassis, C.A.Dimitriadis, K.Papathanasiou, J.Jomaah, G.Ghibaudo, "Analytical unified threshold voltage model of short-channel FinFETs and implementation", *Solid State Electron, vol.64, pp.34-41, 2011.*

[27] Michal Zaborowski, Daniel Tomaszewski, Andrzej, Piotr Grabiec, " Double-fin FETs based

on standard CMOS approach", *Solid State Electron, vol.87, pp.1396-1399, 2010.*

[28] Sung Mo Kang, "CMOS Digital Integrated Circuits Analysis and Design", third edition.

[29] Yannis Tsividis, "Operation and Modelling of The MOS Transistor", second edition.

[30] J.P.Colinge,"Silicon on Insulator Technology", third edition, springer.

J.P.Colinge, "FinFETs and other Multi-Gate Transistors", edition 1, springer, august 2007