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Design for Test and Fault Simulation of Electronic Circuits

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Abstract: *The increasing complexity of circuits and decreasing components size has made the testability and simulation of electronic circuits to be considered crucial and demanding. Therefore, there is need to employ Design for Test (DFT) and fault simulation concepts from the earliest stages of the product design because it impacts all areas of the design of a product from the initial concept to the component choice, investment in test equipments and mechanical design in order to eliminate faults and fabrication defects in the electronic circuits. Furthermore, there is need to design in some circuitry which allows the equipment to test itself (Built-In Self-Test) or allows it to be tested by an external tester (Automatic Testing Equipment). The circuit is simulated to make sure the added test circuitry (BIST or ATE) has not affected the operation of the new circuit. A set of test vectors for the circuit will be written afterwards by the designer if the new circuit passes simulation. A program called a fault simulator is then used to determine the percentage of internal faults that can be detected in the circuit when specified set of test vectors is applied to it. If the test vectors cannot detect an acceptable percentage of faults in the circuits then more test vectors must be written or the circuit must be re-designed so that faults are more detectable.*

Keywords*: DFT, ATPG, BIST, ATE, fault simulation, CUT, DUT.*

1.0 Introduction

The explosive increase in IC complexity was fuelled by the advances in deep sub-micron technology and hence the need for design for test and fault simulation of electronic circuits. Therefore, design for test is used to reduce the manufacturing cost, minimize development time and manage complexity. **(IEE Std 1149.1 (JTAG)** Testability Primer). According to an edition by Ian Poole of Radio-Electronics.com website, Radio and analysis for electronic engineers, testing is a necessary requirement of any production or manufacturing process and it should be employed at the concept stage or the beginning of the product design. These will require a test strategy at an early stage that will determine the type or types of test to be used and also the test systems that will be employed as a result. Also, the type of testers e.g. ATE, will also be considered as another test strategy that will be incorporated into the electronics design at the earliest stages. The test strategy covers the analysis of the product, review available test equipment, review test opportunities, create test strategy document, implement test strategy, collect metrics, review and change test strategy and testing.

Structural test which is considered as the most widely used tool for design for test and fault simulation in the industry today simulates the faults that may exist in the design due to fabrication defects. The idea is to apply suitable digital vectors that will sensitize the faults such that the faulty circuit will produce a different result at the primary output from a fault-free circuit. This requires suitable fault models to be created to model fabrication defects and for these the models to be simulated in the design to identify the right set of digital vectors to apply to the actual fabricated circuit. **(Bushnell and Agrawal, 2000)** Automatic Test Pattern Generation (ATPG) is used to generate the input test pattern or test vector so that when applied to the electronic circuits, enables automatic test equipment to find the target faults**. (Agrawal, 2000)** According to a survey on the Electronic Design Automation for Integrated Circuits by Lavagno, Martin and Scheffer, a fault is said to be detected by a test pattern when testing a device that has only that one fault, is different than the expected output. Inputs test patterns can also be generated by Built-in self-test (BIST) were the input test patterns are generated by on chip logic. **(Stroud, 2002)** This means the chip can test itself without stimulus thus reducing the cost of testing and ATE is no longer needed.

A fault simulator is used to determine and find the percentage of internal faults detected in the electronic circuit when the input test patterns or test vectors are applied to it. Therefore, there is an acceptable percentage of faults the test vectors should detect and should in case it cannot detect the faults, more test vectors would be written or the circuit re-designed to allow for the detection of faults.

2.0 Basic Concepts of Testing and Fault Simulation of Electronic Circuits

Testing is the process of verifying that the fabricated IC functions as expected or designed. The goal of testing is to correctly separate good chips from bad ones. It has two main aspects; controllability and observability as the design modification that provides improved access to internal circuit element. Therefore, the design for test plays an important role in the development of test programs and as an interface for test application and diagnostics. **(Wang, Wu and Wen, 2006)**

2.1 Built-In Self-Test (BIST)

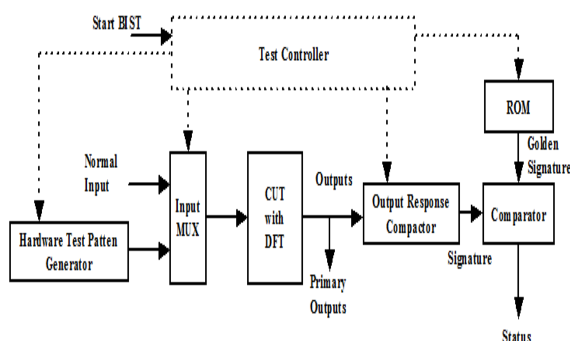
Modern day ICs based on deep sub-micron technology requires the addition of a redundant circuitry where the ICs are tested before each time they are start up. Therefore, testing a circuit every time they start up is called Built-In Self-Test (BIST). **(Bardell, McAnney and Savir, 1987)** The main purpose of BIST is to reduce the complexity and thereby decrease the cost and reduce reliance upon external (pattern-programmed) test equipment. Once the BIST finds a fault, the readjustment in connections to replace the faulty part with a fault free one is a design problem.

2.1.1 Basic architecture of BIST

BIST is basically same as off-line testing using ATE where the test pattern generator and the test response analyzer are on-chip circuitry (instead of equipments). As equipments are replaced by circuitry, so it is obvious that compressed implementations of test pattern generator and response analyzer are to be designed. The basic architecture of BIST is shown in the figure below:

Figure 1: Basic architecture of BIST

The figure 2 above shows the basic architecture of



BIST circuit. It comprises of the following modules; Hardware Test Pattern Generator, Input Mux, Output Response Compactor, ROM, Comparator and Test Controller. The Hardware Test Pattern Generator generates the patterns required to sensitize the faults and propagate the effect to the outputs (of the CUT). The Input Multiplier allows normal inputs to the circuit when it is operational and test inputs from the pattern generator when BIST is executed. Output response compactor performs lossy compression of the outputs of the CUT. Golden signatures that need storing when compared with the compacted CUT response is done by the ROM. The comparator compares compacted CUT response and golden signature (from ROM) whereas the circuit to control the BIST is done by the Test controller.

2.2 Automatic Test Pattern Generation (ATPG)

An ATPG is used to generate an input test pattern that can find the presence or absence of faults at some location in the circuit. It requires the use of an external tester called Automatic Test Equipment (ATE) to test semiconductor devices after manufacture or to assist with determining the cause of failure (failure analysis). Therefore, ATE is used in circuits that do not have an in built tester (BIST). ATPG generates test patterns for faults using fault sensitization, propagation, justification and thermal imaging. The latter involves taking images of the silicon (of the circuit) and then drawing conclusions based on temperature profile of various regions of the silicon. **(Claey, Dilhaire and Quintard, 1994)**

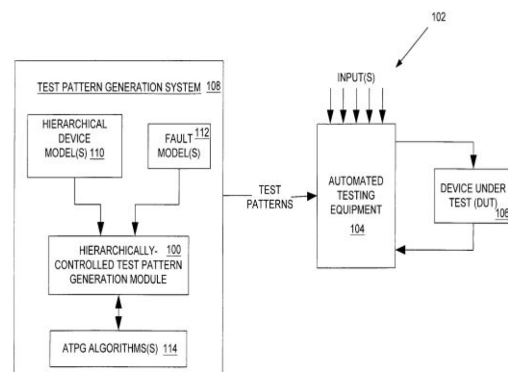


Figure 2: Automatic Test Pattern Generation system for a Device Under Test (DUT)

The figure above shows ATPG system used for testing a Device under Test (DUT). It consists of a fault model (s) 112, Hierarchical Device Model (s) 110, hierarchically controlled Test pattern Generation module 110, ATPG Algorithm(s) 114, Automated Testing Equipment 104 and the Device Under Test (DUT) 106. The APG generates an input test pattern that is used by an Automated

Testing Equipment to test the Device Under Test (DUT).

2.3 Fault simulation

Breadboards has been used over decades for pre-design validations however, it is too cumbersome for large designs. This is the reason while a computer program called a fault simulator is used to simulate the generated test patterns to find undetected faults, calculate the fault coverage, fault diagnosis, test grading, test generation and fault tolerance. A fault simulator is like an ordinary simulator but needs to simulate two versions of a circuit where one is without any fault for a given input pattern while the other is with a fault inserted in the circuit and for the same input pattern. If the outputs under normal and faulty situation differ, the pattern detects the fault. The latter is repeated for all faults. Once a fault is detected it is dropped and is not considered further during fault simulation by random pattern. **(McCalla, 1988)** Serial, parallel and deductive fault simulations are the following fault simulation algorithm used.

2.4 Fault models

Fault model is an abstraction of the real defects in the silicon such that the faults of the model are easy to represent and should ensure that if one verifies that no faults of the model are in the circuit, quality of test solution is maintained. The widely accepted fault model is the stuck-at fault model whereas the others used are delay fault model and bridging fault model. **(Abraham, 1986)**

In stuck-at fault model, the faults are fixed (0 or 1) value to a net which is an input or an output of a logic gate or a flip-flop in the circuit. if the net is stuck to 0, it is called stuck-at-0 (s-a-0) fault and if the net is stuck to 1, it is called stuck-at-1 (s-a-1) fault. In Delay fault model, the fault increases the input to output delay of one logic gate at a time. Whereas in Bridging fault model, short is assumed between two nets in the circuit. The logic value of the shorted net may be modelled a 1-dorminant (OR bridge), 0-dominant (AND) bridge.

3.0 Diagnostics

It is unfortunate fact of life that not all products will work once they have been manufactured and it is necessary to test the product before it is shipped to ensure that it is operational. Since it has been stated that it is not uncommon for chips arriving at a test floor for the first time to fail or exhibit a zero-yield situation, the chip will have to go through a debug process which identify the reason for the zero-yield situation. In some conditions the percentage of test fails or test fall-out are higher than the expected or acceptable and again the chips will be subjected to an analysis that will ascertain the reasons for the test fall-out.

The fail log is then used in cases where vital information about the nature of underlying problem is hidden in the way the chips fail during test. Here, additional fail information beyond a simple fail/pass is collected into a fail log to facilitate better analysis. The fail log contains information on when (e.g. tester cycle), where (e.g. at what tester channel) and how (e.g. logic value) the test failed. A diagnostic process attempts to get from the fail log the logical/physical location inside the chip were the problem most likely started and then several volume diagnostics which involves running large number of failures to determine the systematic failures occurs afterwards. Furthermore, for devices such as Printed Circuit Board, Multi-Chip Modules and embedded or stand alone memories, diagnostics can identify the failing unit and create a work order for solving and repairing the failing unit.

4.0 Scan design

Scan design delivers test data from chip inputs to internal Circuit under Test (CUT) and monitors their output. It does this with the use of its registers (flip-flops or latches) which are connected to one or more scan chains were it gains access to internal nodes of the chips. The test patterns and the results of the functional clock signals pulsed are transmitted to the chip output pins were they are compressed to the good results. The scan design processes a test compression technique that decompresses the scan input on chip and compresses the test output. scan design output are provided in forms such as Serial Vector Format (SVF), to be executed by test equipments.

5.0 Conclusion

As far as IC malfunction due to instabilities, defects and fault, the design for test and fault simulation cannot be overemphasized. It plays an important role in the development of test programs and as an interface for test application and diagnostics. It is a key element in the design of any product which is considered right from the concept stage of the product in order to reduce the production cost, eliminate the fabrication defects and faults in the circuit. ATPG generates necessary test vectors which enables an ATE to test the device under test. Whereas some circuit have Built-

In Self-Test (BIST) circuitry so that the unit has complete internal test each time the power is turned on. A computer program called a fault simulator is used in detecting the percentage of internal faults that can be detected in the circuit when a specified set of test vectors is applied to it.

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