

# Signal Processing Segmented Serial Parallel Multiplier Using VLSI

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**Abstract** In this paper a novel VLSI SP oriented architecture for implementation of serial parallel Multipliers (SPM) is proposed. The VLSI oriented multiplier is based on a segmentation technique of SPM and the conventional full adders are replaced by low power full adder. In this paper two architectures namely Segmented Based SPM, Folded VLSI oriented segmented based SPM are compared for power and area. The proposed VLSI SP oriented architecture achieves higher throughput and less area compared to the segmentation based serial parallel multiplier proposed (1). The proposed VLSI SP oriented architecture permits the optimization of the area, speed and power.

## 1. Introduction

Segmentation based architecture [1] is shown in Figure 1. The architecture is efficient in throughput and speed. The new proposed architecture i.e. VLSI SP oriented architecture uses VLSI Signal Processing concepts like folding to minimize the hardware resources. The hardware resources can be reduced by increasing the input clock frequency. In this paper the proposed architecture for 4 bit operand multiplication is implemented in Cadence for functionality verification. Sixteenbit, four-tap FIR is implemented in veri log for power and area comparison. The segmentation based architecture requires 5 full adders. The VLSI SP oriented segmentation based architecture requires 3 full adders almost 5.5% hardware is reduced by increasing only the input clock frequency. Increasing the input clock frequency is easier. The segmentation based SPM [1] uses two blocks MB 1 and MB2. It segments the computation i.e. the lower bits and the upper bits of Product is computed in different segments or blocks. The resultant products are given on two line Ph (upper bits) and PI (lower bits). The pi will be valid for m+q cycles where q is the number of bits in each segments and m is the number of serial input bits. The remaining bits of the product from the Ph are valid. The segmentation based architecture for serial parallel multiplier for n=6 bits, k=2 blocks and q=3 bits is shown in Figure 1.

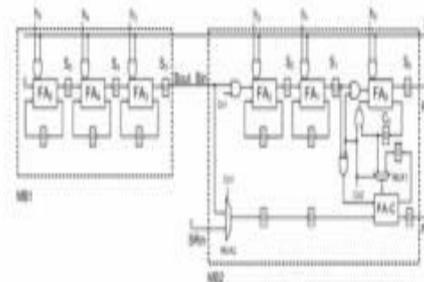


Figure 1 Segmentation based architecture for the serial parallel multiplier for n=6 bits, k=2 blocks, q=3 bits

Timing diagram of the segmentation based SPM is shown in figure 2. The segmentation block MB 1 and MB2 can be extended to more number of bits as shown in Figure 3.

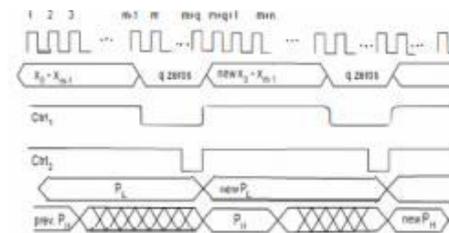


Figure 2 Timing diagram for segmentation based SPM

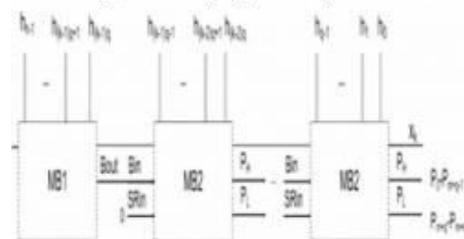


Figure 3 Segmented SPM blocks extended to more number of parallel bits

## 2. SEGMENTATION BASED SPM

The Proposed SPM uses the folding concepts of VLSI SP. The folding transformation is used to systematically determine the control circuits in DSP architectures where multiple algorithm operations (such as addition operations) are time multiplexed to a single functional unit (such as pipelined adders). By executing the algorithm operations on a single functional unit, the number of functional units in the implementation is reduced resulting in an integrated

circuit with low silicon area. This architecture helps to minimize the area of SPM and also the resources. Only the clock speed has to be doubled (depending on the number of folding N). The proposed VLSI SP architecture saves 5.5% of the resources compared to the segmentation based SPM proposed in [1] for 4 bit multiplication. The proposed VLSI SP oriented Segmentation based SPM architecture is shown in Figure 4. Where each block contains only one full adder

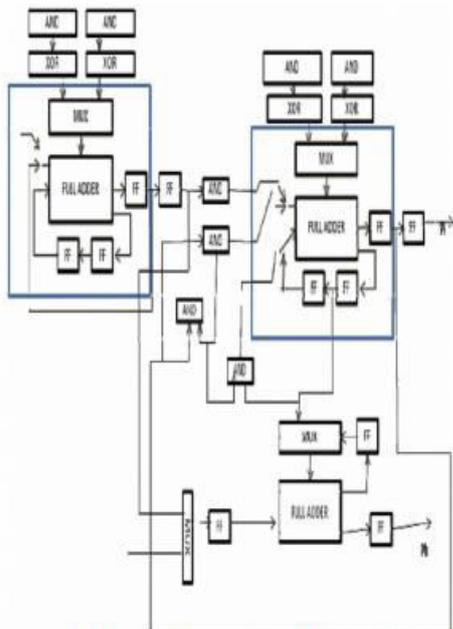


Figure 4 VLSI SP oriented Segmentation based SPM architecture

The VLSI SP Oriented segmentation based proposed architectures consist of I Full adder in each block that is only I computational full adder in MB1 block and MB2 block. The architecture also requires One full adder for Ph output path in MB2 blocks. The proposed VLSI architecture folds the two full adders present in block MB I into one full adder and the two full adders present in block MB2 to one full adder (two full adder folded to reduce the resource) for a 4-bit operand multiplication. The folding is done using multiplexers or MOSFET acting as switches. The inputs to the full adder are switched depending on the select line of the multiplexer. The delay flip flops are introduced based on the formula.

$$D_f(U \rightarrow V) = N w(e) - P_u + v - u$$

Where

U = source node

V = destination node

$P_u$  = the computation time of the source node.

$D_f(U \rightarrow V)$  = folded delay obtained by folding the edges (U → V).

u = folding set value of the source node.

v = folding set value of the destination node.

The segmentation based SPM has two blocks i.e. MB I and MB2, for 4 bit multiplier. The first 6 clock cycle the PI output is valid and the next 2 clock

cycles Ph output is valid. The segmentation based SPM requires 1018 transistors for 4 bit serial parallel multiplication. As the number of bits increases the number of transistors also increases. The resource computed for 4 bit segmentation based SPM is given in Table 1.

MB1	No of gates required	No of transistors required for each gate	Total
AND gate	2	6	12
XOR gate	2	22	44
Full Adder	2	74	148
D-FlipFlop	4	50	200
MB2			
AND gate	6	6	36
XOR gate	2	22	44
Multiplexer	2	5	10
Full Adder	3	74	222
D-FlipFlop	6	50	300
Inverter	1	2	2
		<b>Total</b>	<b>1018</b>

Table 1 Resource computation for Segmentation based SPM

MB1	No of gates required	No of transistors required for each gate	Total
AND gate	2	6	12
XOR gate	2	22	44
Multiplexer	2	5	10
Full Adder	1	74	74
D-FlipFlop	5	50	250
Inverter	1	2	2
MB2			
AND gate	6	6	36
XOR gate	2	22	44
Multiplexer	5	5	25
Full Adder	2	74	148
D-FlipFlop	5	50	250
Inverter	2	2	4
		<b>Total</b>	<b>899</b>

Table 2 Resource computation for VLSI SP oriented Segmentation based SPM

The VLSI SP oriented segmentation based SPM requires 899 transistors for 4 bit serial parallel multiplication. As the number of bits increases the number of transistors also reduces as compared to Segmentation based SPM. The resource computation for 4 bit VLSI SP oriented segmentation based SPM is given in Table 2. The dynamic power consumption of the segmentation based SPM was found to be 1.78 mW and the dynamic power consumption of the VLSI SP oriented segmentation based SPM was 2.4595 mW.

### 3. Implementation in Cadence tool

The segmented based SPM and the VLSI SP Oriented (folded) segmentation based SPM are implemented in cadence tool and the results are compared. The top level schematics of segmentation based SPM is shown in Figure 5. The transient

analysis of the VLSI SP oriented Segmentation based SPM implemented in cadence is shown Figure 6.



Figure 5 Segmented based SPM implemented in Cadence



Figure 6 Results of VLSI SP oriented Segmentation based SPM in Cadence

The VLSI SP oriented architecture with folding concepts applied and the schematics of VLSI SP oriented segmented SPM implemented in Cadence is shown in Figure 7. The folding is done using multiplexers. The transient analysis of the VLSI SP oriented segmentation based SPM implemented in cadence is shown in Figure 8

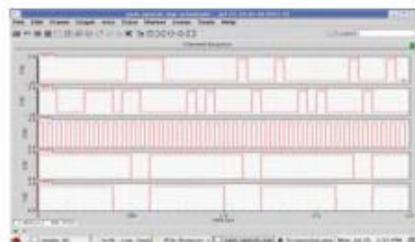


Figure 8 Results of VLSI SP oriented segmentation based SPM in Cadence.



Figure 7 Schematics of VLSI SP oriented segmented SPM implemented in Cadence

The VLSI SP oriented segmentation based SPM and the Segmentation based SPM are implemented using Virtex II Pro FPGA XC2VP20 FFI152 for comparison of the hardware resources in FPGA. The top level VHDL code implemented for the MB 1 block of the segmentation based SPM is shown in figure 9. Similarly the MB2 block is also implemented which is not shown here. The top level code consists of both MB 1 and MB2. The device

summary for the same after place and route is shown in Table 3. The RTL schematics obtained for the segmentation based SPM for the VHDL code implemented in Xilinx ISE 9.1 is shown in figure 9. The device summary for the same after place and route is shown in Table 3.



Figure 9 RTL Schematics of Segmentation based SPM

Number of BUFGMUXs	1 out of 16	6%
Number of External IOBs	10 out of 564	1%
Number of LOCed IOBs	0 out of 10	0%
<b>Number of SLICES</b>	<b>8 out of 9280</b>	<b>1%</b>

Table 3 Device Utilization Summary of Segmentation based SPM

The RTL schematic for the VLSI SP oriented segmentation based SPM implemented in Xilinx ISE 9.1 is shown in figure 11. The device summary of the same is shown in figure 12. The figure 13 shows the output obtained from simulation of the VHDL code for VLSI SP oriented Segmentation based SPM. The simulator used is ISE Simulator



Figure 10 RTL Schematics for the VLSI SP oriented segmentation based SPM as obtained from Xilinx ISE 9.1

Number of BUFGMUXs	1 out of 16	6%
Number of External IOBs	11 out of 564	1%
Number of LOCed IOBs	0 out of 10	0%
<b>Number of SLICES</b>	<b>6 out of 9280</b>	<b>1%</b>

Table 4 Device Utilization Summary for VLSI SP oriented segmentation based SPM

#### 4. Hardware implementation of Proposed SPM as FIR

The Segmentation based SPM and VLSI SP oriented segmentation based SPM are implemented as 4- tap, 16 bit FIR, using design vision tool from Synopsys for comparison of power. The two architectures are implemented in VERILOG. The

area comparison in done by making the layout of the two architectures using SOC Encounter tool of Cadence. The leakage power consumption of segmented based SPM was found to be 6.6340uW. The leakage power consumption of VLSI SP oriented segmented based SPM was found to be 8.5064uW. Figure 12 shows the comparison of leakage power of the two SPM architectures

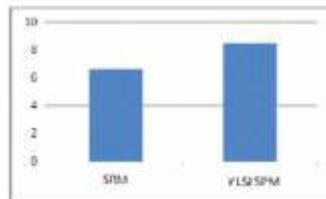


Figure 12 Leakage power comparisons of the two architectures

The Dynamic power consumption of segmented based SPM was found to be 4.5967mW. The Dynamic power consumption of VLSI SP oriented segmented based SPM was found to be 4.9429mW. Figure 13 shows the Dynamic power comparisons of the two SPM architectures..

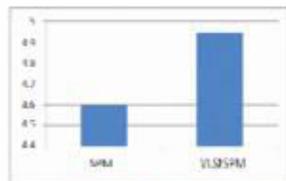


Figure 13 Dynamic power comparisons of the two architectures

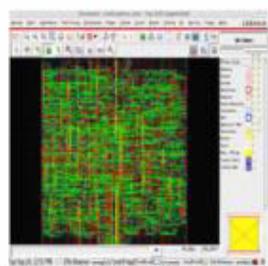


Figure 14 Layout of segmented based SPM in SOC encounter

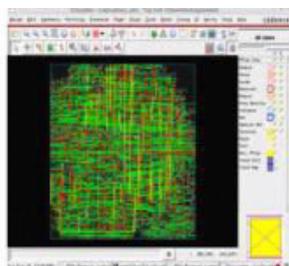


Figure 15 Layout of VLSI SP oriented segmentation based SPM in SOC encounter

Figure 14 figure 15 shows the layout of the two architectures of SPM. It can be seen that the proposed VLSI SP oriented Segmentation based SPM occupies less area. Figure 16 shows the area comparison of the two architectures based on the device summary report obtained from

SOC encounter. It can be seen from the report that area occupied by Segmented based SPM was  $6.6253 \times 10E4$  urn sq. The area occupied by VLSI SP oriented segmentation based SPM was  $6.392 \times 10E4$  urn sq. Table 5 shows the Area comparison of the two architectures of SPM. It can be seen that VLSI SP oriented segmentation based SPM occupies 5.5% less area compared to segmented based SPM for 4-tap 16 bit FIR. Figure 16 shows the Area occupied by two SPM architectures. Table 5 shows the area comparison .



Figure 16 Area Comparison of two architectures of SPM

Architecture	Area Estimate	Remarks
Segmentation based SPM	$6.6253 \times 10E4 \mu m$	
VLSI Oriented Segmentation based SPM	$6.392 \times 10E4 \mu m$	5.5% Less area

Table 5 Area comparison of the two architectures for 4-Tap 16 bit FIR

## 5. Conclusion and Future work

This paper describes a multiplier that has the desirable characteristics which will make it useful in a variety of VLSI oriented signal processing applications. Its capability to handle two's complement positive and negative numbers makes it compatible with standard hardware and standard data formats. The data throughput rate is approximately same as rate of the segmentation based serial parallel multiplier from which it is constructed. Further folding of Multipliers can be done to reduce the hardware complexity. The proposed VLSI SP oriented Segmentation based Serial Parallel Multiplier can be used in any image processing, signal processing or Biomedical applications. It gives the advantage of low area and improved speed as compared to the conventional FIR. Cut set retiming can be used to reduce the critical time.

## 5. References

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