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A Novel Low Power Full Adder Design

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Abstract - *Achieving high speed integrated circuits with low power consumption is a major concern for the VLSI designers. The advancement in VLSI technology has contributed to portable and handheld devices such as mobile and laptop. These devices need low power consuming elements. Most arithmetic operations are done using adder, which is the major power consuming element in the digital circuits. The adder is a basic building block of many VLSI applications such as Digital Signal Processor, Microprocessor, cache memory, ALU and Multipliers. The primary objective of our project is to design a modified low power full adder. We have designed a new two transistor XOR circuit(2T XOR) using pass transistor logic. This two transistor XOR circuit provides better performance than the previous existing 2T XNOR circuit. In addition to 2T XOR we have designed an eight transistor full adder using this proposed XOR logic . This 8T full adder consists of proposed 2T XOR, 2T MUX, and 2T XNOR circuits. The performance of this full adder is compared with existing 8T full adder and the significant improvement is achieved in power consumption. The circuit functionalities are verified through the simulation using Tanner EDA Tool v14.1.*

1. Introduction

The advantage of utilizing a combination of low-power components in conjunction with low-power design techniques is more valuable. Requirements for lower power consumption continue to increase significantly as components become battery-powered, smaller and require more functionality. In the past the major concerns for the VLSI designers was area, performance and cost. Power consideration was the secondary concerned.

Now a day's power is the primary concern due to the remarkable growth and success in the field of personal computing devices and wireless communication system which demand high speed computation and complex functionality with low power consumption. The motivations for reducing power consumption differs from application to application. The main reason for using micro powered battery in portable applications like cell phones are to keep the battery lifetime and weight reasonable and packaging cost low.

For high performance portable computers like laptop aims to reduce the power consumption of the electronics portion of the system. Finally for the high performance non battery operated system such as workstations the overall goal of power minimization is to reduce the system cost while ensuring long term device reliability. For such high performance systems, process technology has driven power to the fore front to all factors in such designs.

At process nodes below 100 nm technology, power consumption due to leakage has joined switching activity as a primary power management concern. There are many techniques that have been developed over the past decade to address the continuously aggressive power reduction requirements of most of the high performance.

3. Literature Survey

In recent years a lot of research work has been carried out ([3], [9], [19], [22]) to reduce the power consumption of the full adder. In [3], the 1 bit adders were designed using 10, 8 and 6 transistors with different equations for sum and carry. The adder designs considered in this paper are SERF adder, CLRCL adder, 8T adder and 6T adder. The comparison was done with respect to power, delay and area. The adder designs were checked for their robustness by varying supply voltage and temperature. In [19], a new 9T 1-bit full adder was designed. The main objective of this paper is full output voltage swing, low power consumption and temperature sustainability. Their proposed design is more reliable in terms of power consumption, Power Delay Product (PDP) and temperature sustainability as compared to the existing full adder designs.

The design has been implemented in 45nm technology on Tanner EDA Tool version 13.0. The simulation results demonstrate the power consumption, delay and power delay product at different input voltages ranging 0.4V to 1.4V.In their full adder, 3T XOR gate and a multiplexer are used to implement Sum and one multiplexer is used to implement the Carry. The selector circuit of the

output multiplexers is output of first stage XOR. Therefore, the operation of Sum and Carry output was based on implementation of XOR operation between the inputs B and $C_{in.}$ Simulations have been performed using Tanner EDA Tool version 13.0 at 45nm technology with the input voltage ranges from 0.4V to 1.4V in step of 0.2V. In order to prove that their design consumes less power, have better temperature sustainability and better performance at various input voltages and temperature, simulations are carried out for power consumption and delay and results the PDP. In [22] a 3 transistor XNOR gate is designed. This XNOR logic gate is designed using CADENCE EDA tool and simulated using the SPECTRE VIRTUOSO at 180 nm technology. It is observed that the power consumption is reduced by 65.19 % for three transistor XNOR gate and 48.11% for eight transistor full adder. It is also observed that the delay is reduced by 31.82% for three transistors XNOR gate and 28.76% for eight transistors full adder. They measured the total power is the combination of two main components. They are static power and dynamic power. Finally they concluded that the design proposed for XNOR gate using 3 transistors, full adder using eight transistors has better performance in terms of delay and power. And also in this paper, they have designed four bit Ripple carry adder and it is mapped into Cadence Encounter(R) RTL Compiler Version v14.20-s013_1.In our proposed work a modified 2T XOR circuit is designed. In addition to 2T XOR, a low power 8T full adder is also designed, which consumes less power than the existing 8T full adder.

The rest of the paper is organized as follows: Section 4 discusses the previous work. Section 5 presents the architecture of the proposed full adder and section 6 decribes about software used. The results and discussion are summarized in section 7 and finally section 8 concludes the paper.

4. Existing System

4.1 Basic Full Adder Design

A full adder contains three inputs and two outputs. And it is also known as basic adder. The full adder comprises of two half adders.

4.1.1 Basic Half Adder

A half adder consists of two inputs and two outputs. A and B are the inputs and the outputs are Sum and Carry.

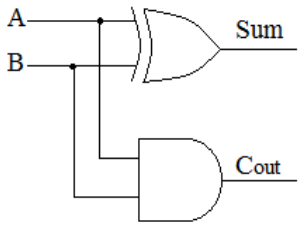

Figure 1. Logic diagram

Table 1. Truth table of an Half adder

INPUT		OUTPUT	
A	B	Sum=A⊕B	Carry=A.B
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The sum and carry equations of an half adder are

Sum = a'b+ab'=a⊕b ---(1)

Carry = ab ---(2)

A full adder can be designed using two half adders and one OR gate. The inputs given to the full adder are a, b, and c. And the outputs are sum and carry.

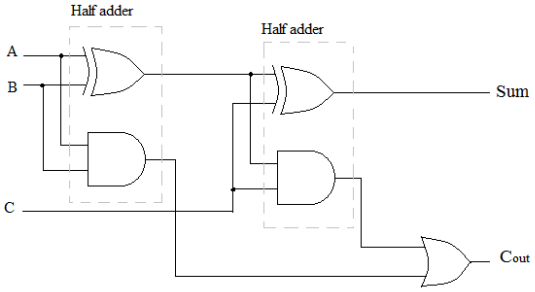

Figure 2. Logic diagram of a full adder using half adders

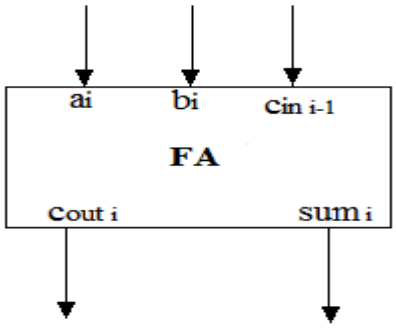

Figure 3. Logic symbol of a full adder

Table 2. Truth table of a full adder

INPUT			OUTPUT	
A	B	C	Sum = A⊕ B⊕C	Carry = A.B + C. (A⊕ B)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The sum and carry equations of a full adder are

Sum = a'b'c+a'bc'+ab'c'+abc ---(3)

Carry = ab+ac+bc ---(4)

A full adder is also known as sequential adder because the inputs are given in a sequential order and this adder is faster than the other adders for a few bit numbers and becomes bit slower when comes to the higher bits.

4.2 Three Transistor Xnor Gate

The XNOR gate (sometimes, EXNOR, ENOR, and, rarely, NXOR, XAND) is a digital logic gate whose function is the logical complement of the exclusive OR (XOR) gate. A high output (1) results if both of the inputs to the gate are the same. If one but not both inputs are high (1), a low output (0) results.

Table 3. Truth table of XNOR logic gate

INPUTS		OUTPUT
A	B	Y = A ʘ B
0	0	1
0	1	0
1	0	0
1	1	1

The XNOR gate with inputs A and B implements the logical expression

A.B + A′ B′ = AʘB ----(5)

A three transistor XNOR is used in the design of a full adder. The following diagram shows 3T XNOR gate.

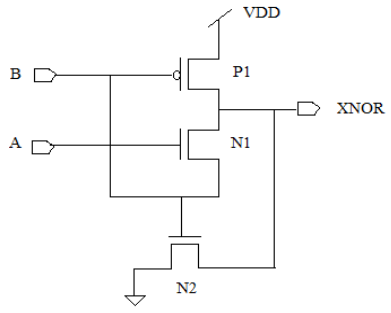

Figure 4. 3T XNOR gate

4.3 Existing Full Adder

This full adder is designed using two numbers of 3T XNOR logic gate and a two transistor multiplexer. This full adder was designed based on the following sum and carry equations.

Sum = A ⊕ B ⊕ Cin ---(6)

Cout = AB + Cin (A⊕ B) ---(7)

The above two equations gives sum and carry output of an existing full adder circuit.

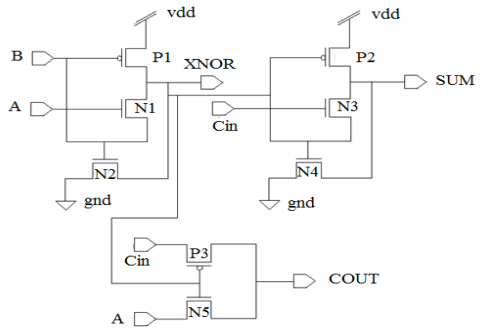

Figure 5. Existing 8T Full adder

Design of three transistor XNOR logic gates are part of full adder so that the number of transistor to design the full adder is reduced. This full adder is implemented using Tanner EDA tool version (v14.1).

Figure 6 clearly explains the structure of an existing full adder circuit.

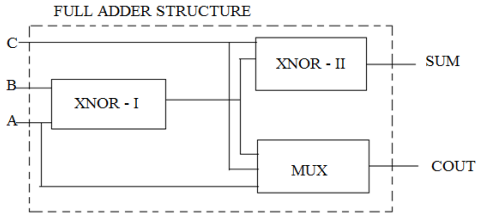

Figure 6. Block diagram of existing full adder

The figure 7 shows the schematic diagram of eight transistor full adder, and for the entire input pattern the output logics are verified. This full adder is designed using Tanner EDA tool version 14.1 and it is designed in 250nm technology. The truth table was verified with this diagram. This full adder consists of three inputs a, b, c and the two outputs are sum and carry. The schematic diagram is designed with the help of S – Edit and the simulated output is obtained with the help of TSPICE.

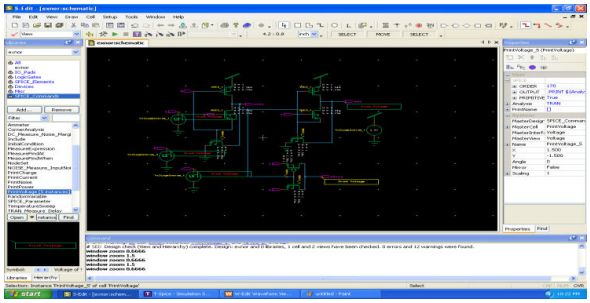

Figure 7. Schematic diagram of an existing full adder

5. Proposed System

In the following sections, the proposed design of the full adder is presented and the simulation results are given and discussed. Further a comparison and evaluation for proposed and existing designs are carried out.

The proposed full adder consists of XOR logic gate, XNOR logic gate and a 2:1 multiplexer. In this adder, a new XOR is designed using pass transistor logic which overcomes the disadvantages of existing XNOR logic gate. This full adder is a combination of existing 2T XNOR logic gate and a proposed 2T XOR is called as XOR – XNOR FULL ADDER.

5.1 Proposed 2t Xor Logic Gate

The XOR gate is a digital logic gate that gives a true (1/HIGH) output when the number of true inputs is odd.

An XOR gate implements an exclusive or; that is, a true output results if one, and only one, of the inputs to the gate is true. If both inputs are false (0/LOW) or both are true, a false output results.XOR represents the inequality function, i.e., the output is true if the inputs are not alike otherwise the output is false.

The XOR gate functions are shown in the table and denoted by this ⊕ . The logic expression for XOR is:

$$A \oplus B = A'B + AB' \qquad \text{---- (8)}$$

Table 4. XOR Gate function

INPUTS		OUTPUT
A	B	Y = A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

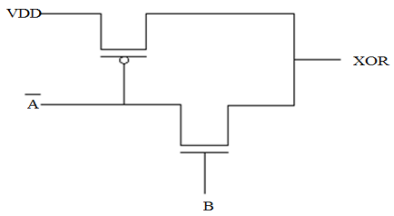

Figure 8. Proposed 2T XOR logic gate

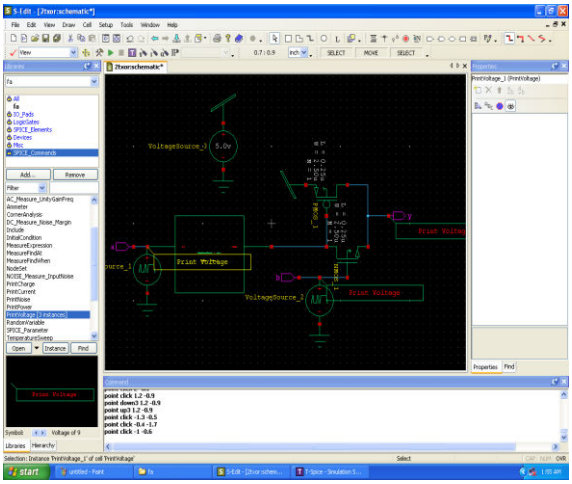

Figure 9. Schematic diagram of proposed full adder

5.2 PROPOSED FULL ADDER

As shown in the below figure 10, the 8T full adder contains three modules one 2T XOR gate, one 2T XNOR gate and a 2-transistor multiplexer (2T MUX). Owing to the appealing traits of a small number of transistors and a mere 2-transistor (2T) delay, it can work at high speed with low power dissipation.

By using proposed 2T XOR gates we are able to minimize the transistor count of the full adder and subsequent decrease in power and delay. The sum output is basically obtained by a cascading XNOR with XOR. The carry output is obtained in accordance with above mentioned equation (10).

The final sum of the products is obtained using a wired XNOR logic. It is quite evident from figure 10 that two stage delays are required to obtain the sum output and at most two stage delays are required to obtain.

By creating a comparison table we can observe that how much delay and power has been reduced by using proposed 2T XOR gate.

The logical function of the 1 bit full adder operation equations presented below can be stated as follows: given the inputs A, B and C which calculate two 1-bit outputs Sum, for sum and Cout, for carry out.

5.3 Proposed Full Adder Design

$$Sum = A \oplus B \oplus C \quad \text{---- (9)}$$

$$Carry = AB + C (A \oplus B) \quad \text{---- (10)}$$

This Full adder is designed using one 2T XOR logic gate, one 2T XNOR logic gate and a 2:1 multiplexer which consumes less power than existing full adder circuit. The proposed system with 2T XOR gate, 2T XNOR gate and a 2:1 MUX is simulated using T- spice in Tanner Tools. All the results are obtained in 250nm CMOS process technology with a 5V supply voltage.

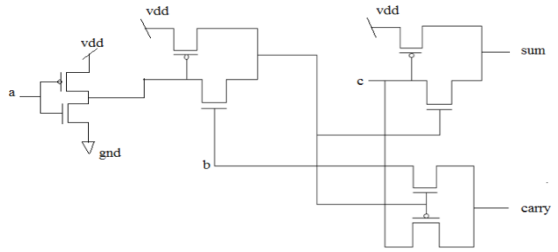

Figure 10. Proposed 8T full adder

The following diagram shows proposed full adder using XOR and XNOR logic gates. In general, existing full adders are XOR – XOR full adder and XNOR – XNOR full adder. We have designed a XOR – XNOR full adder which consumes less power than the XNOR – XNOR full adder.

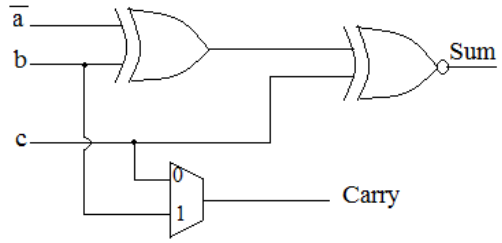

Figure 11. Logic diagram of proposed full adder

In order to establish an impartial simulation circumstance, the input patterns are obtained, which covers every possible inputs combination of A, B and C.

The delay has been measure between the time when the changing input reaches 50% of voltage level to the time it output reaches 50% of voltage level for both rising and fall transition for Sum and Cout. The power delay product (PDP) is measured as the product of the average delay and the average power. The following block diagram clearly explains the structure of a proposed full adder.

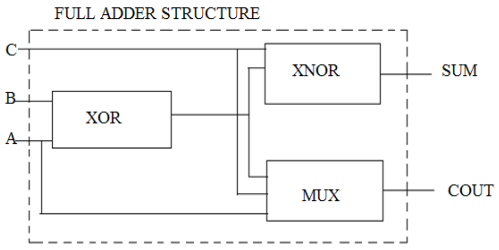

Figure 12. Block diagram for proposed full adder

The schematic diagram of a proposed full adder is designed. Using S – Edit in Tanner EDA tool version 14.1.The simulations are verified using T – SPICE.

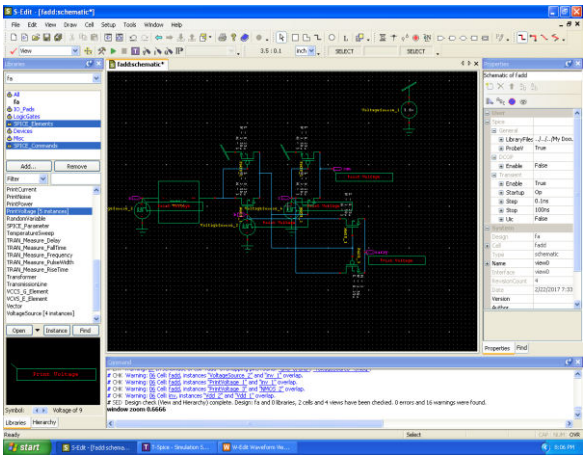

Figure 13. Schematic diagram for proposed full adder

6. Software Details

6.1 Tanner Eda Tool V14.1

Today's semiconductors and electronic systems are complex, that designing them would be impossible without electronic design automation (EDA). Electronic design automation (EDA), also referred to as electronic computer-aided design (ECAD), is a category of software tools for designing electronic systems such as integrated circuits and printed circuit boards. The tools work together in a design flow that chip designers use to design and analyze entire semiconductor chips. Since a modern semiconductor chip can have billions of components, EDA tools are essential for their design.

Current digital flows are extremely modular (Integrated circuit design, Design closure, and Design flow (EDA)). The front ends produce standardized design descriptions that compile into invocations of "cells", without regard to the cell technology. Cells implement logic or other

electronic functions using a particular integrated circuit technology. Fabricators generally provide libraries of components for their production processes, with simulation models that fit standard simulation tools. Analog EDA tools are far less modular, since many more functions are required, they interact more strongly, and the components are (in general) less ideal.

EDA for electronics has rapidly increased in importance with the continuous scaling of semiconductor technology. Some users are foundry operators, who operate the semiconductor fabrication facilities, or "fabs", and design-service companies who use EDA software to evaluate an incoming design for manufacturing readiness. EDA tools are also used for programming design functionality into FPGAs.

6.2 Tanner Design Tools

Tanner EDA is mainly used to analyze circuits at switch level & gate level.

S-edit - A schematic capture tool

T-spice - the SPICE simulation engine integrated with S-edit

W-edit - Waveform formatting

6.2.1 S-Edit

S-Edit is a powerful design capture & entry tool that can generate net lists directly usable in T-Spice simulations. Provides an integrated environment for editing circuits, setting up and running simulations and probing the results. It also provides the ability to perform SPICE simulations of the circuit.

6.2.2 T-Spice

It is a complete design capture and simulation solution that provides accuracy. The role of T-Spice is to design and verify a circuit's operation. T-Spice simulation results allow circuit designers to verify and fine-tune designs before submitting them for fabrication. Performs fast, accurate simulations for analog and mixed-signal IC designs and fully supports foundry models for reliable and accurate simulations.

7. Result And Discussions

Tanner EDA offers a complete design environment for analog, mixed signal or MEMS domains in one highly-integrated end-to-end flow. Similar design is followed for all regular, modified and proposed FULL ADDER. Figure 15 which exhibits the simulation results of the proposed FULL ADDER structure in terms of transistor count, power.

In this project simulation results are obtained using Tanner EDA Tools version 14.1.

7.1 Implementation Results

The implementation result is obtained by using Tanner S-Edit Tool (version 14.1). The simulation results are as follows:

The figure 14 represents the output power of an existing full adder designed with eight transistors. This simulated waveform satisfies the truth table of a full adder.

This Figure 15 represents the power output of proposed full adder which is generated using T – SPICE in Tanner EDA Tool v14.1.From fig 19 and 20 we can infer that the power consumed by the proposed 8T full adder is less than the power consumed by the existing 8T full adder.

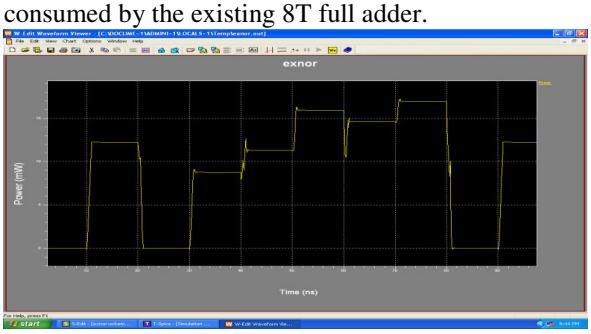

Figure 14. Power output for an existing full adder

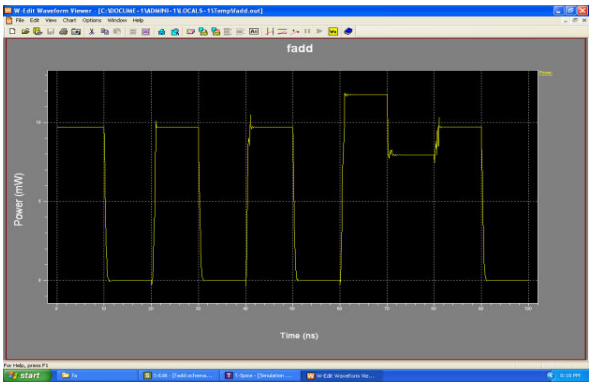

Figure 15. Power output of proposed full adder

Table 5. Comparison table

PARAMETER	EXISTING SYSTEM	PROPOSED SYSTEM
TRANSISTOR COUNT	8	8
POWER (mW)	12.5	9.5

8. Conclusion

In this proposed work, a new 2T XOR is designed using pass transistor logic and a simple low power 8T full adder is designed using the proposed 2T XOR gate, 2T XNOR gate and 2T multiplexer. The extensive simulations were carried out using Tanner EDA 14.1. This full adder is implemented in 250nm CMOS technology to evaluate and compare the performance of proposed 8T full adder and the existing 8T full adder.

Both the full adders are compared in terms of power consumption. The power consumption of

existing 8T full adder is 12.5mW. The power consumption of our proposed 8T full adder is 9.5mW. From the simulation output we can infer that the power consumed by the new proposed 8T full adder is less than the power consumed by the existing 8T full adder.

The result analysis shows that the proposed structure is better than the existing full adder circuit in terms of power.

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