A Review On: Linearization Technique for Operational Transconductance Amplifier

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Abstract: Transconductors are basic building blocks found in many analog signal processing circuits such as continuous time filters, voltage controlled oscillators and current sensing circuits. Linearity is a crucial factor in designing transconductor. Several methods are adopted to improve the linearity of the transistor. One of the method that is used to improve the linearity of the transistor is source degeneration. An improved performance can be observed when a degenerated auxiliary differential pair is used to drive the bulk of main differential pair, which reduces distortion and increases the linear input range of a differential pair with source degeneration.

Introduction

Transconductors are important building block in analog signal processing circuits such as continuous time filters, voltage controlled oscillators and current sensing circuits [2,3]. A block that converts a specific range of input voltage to output current is known as transconductor Gm and hence it is voltage controlled current source (VCCS) [1]. In designing delta-sigma modulators for high resolution Analog-digital converters, Linearity is the most crucial requirement to accomplish required signal to noise ratio [1,2,3]. The CMOS devices are best suited for transconductor design because it has less power requirements. In operational transconductor amplifier (OTA), the input circuitry is same as that found in many modern op-amps. The remainder of OTA is composed of current mirrors of unity current gains. The major controlling factor in the OTA is the external bias current Iext. The output current of OTA and transconductance Gm are also controlled by this current. The attractive properties of OTA are fast speed and bias dependence transconduance programmability [5]. While designing an OTA, many factors are to be considered such as linear input range[7], control voltage of transconductor, symmetry of the two differential outputs,[7,8] etc. When the control voltage of the OTA is increased, it increases the transconductance but limiting the input voltage range and thus increasing the supply voltage. Hence, it is critical in designing transconductor with low supply voltage.[8] If the two differential outputs are not symmetric then it corresponds to common mode distortion that occurs at the output. There are two types of modes in designing a differential transconductor, depending on operation of input transistors. triode mode transconductor and saturation mode transconductor.[1,7,8] Triode mode has better linearity while saturation mode has better speed performance. Saturation mode transconductor exhibits moderate linear performance.

Several design techniques for improving the linearity of transconductor has been reported in literature. The methods for improving linearity are [2,3]source degeneration using resistors, [7]cross-coupling of multiple differential pair, [8]constant drain-source voltages, adaptive biasing, [11]class AB configuration,[6] pseudo differential stages and shift level biasing. Source degeneration using resistors requires large resistor for wide linear input range. The class AB configuration achieves low power consumption but the linearity is extremely degraded. The cross coupled differential pair is sensitive to PVT variations. The source degeneration technique decreases the effective transconductance and increase the noise due to lower transconductance and addition of resistors.

1. Literature Review on Linearisation Techniques

1.1 Transconductor using source degeneration

A simple differential transconductor is shown in Figure 1.1.(a). Assuming that M1 and M2 are in...
saturation and perfectly matched, the drain current is given by

\[ I_D = \frac{\mu C_E}{2} (V_{GS} - V_T)^2 \]

The transfer characteristics are given by:

\[ I_{OUT} = I_{out1} - I_{out2} = \sqrt{2\mu C_E} V_i \sqrt{1 - \frac{V_i^2}{4(V_{GS} - V_T)^2}} \]

\[ \approx \sqrt{2\mu C_E} V_i \cdot \frac{1}{2} \sqrt{\frac{1}{\beta_n I_b}} \cdot \sqrt{2\mu C_E B_n I_b} \cdot V_i \]

\[ = A \cdot V_i \cdot B \cdot V_i \cdot V_i \]

\[ A = \frac{1}{2} \sqrt{2\mu C_E} \]

\[ B = \frac{1}{2} \sqrt{\frac{1}{\beta_n I_b}} \]

\[ G_m = \sqrt{2\mu C_E} \]

\[ \text{HD}_3 = \frac{1}{82} \left( V_{GS1} - V_{GS2} \right)^2 \]

where \( V_i = V_{In1} - V_{In2} \). If \( V_{GS} \) is large enough, the higher linearity can be achieved. Unfortunately, it cannot be used in the low-voltage application and the linear input range is limited. Simplest techniques to linearize the transfer characteristic of MOS transconductor is the one with source degeneration using resistors as shows in Figure 1.2.(b). The circuit is described by

\[ V_i - RI_{OUT} = V_{GS1} - V_{GS2} \]

where \( R \) is the resistor used for source degeneration. The transconductance \( G_m \) is

\[ G_m = \frac{gm}{1 + gmR} \]

where \( gm \) is the transconductance of transistor \( M1 \) and \( M2 \). It should be noticed that the nonlinear term depends on \( V_i - RI_{OUT} \) rather than \( V_i \). Higher linearity can be achieved when \( R >> 1/gm \). The disadvantage of this transconductor is that large resistor value is needed in order to maintain a wider linear input range. Owing to \( G_m = 1/R \), the higher transconductance is limited by the smaller resistor. Hence, there is a tradeoff between wide linear input range and higher transconductance which is mainly determined by a resistor.

1.2 Transconductor using regulated cascode to replace auxiliary amplifier

In Figure 1.2.(a), regulating amplifier keeps \( V_{DS} \) of \( M1 \) at a constant value determined by \( V_C \). It is less than the overdrive voltage of \( M1 \). The voltage can be controlled from \( V_C \) so as to place \( M3 \) in current-voltage feedback, thereby increasing output impedance. The concept is to drive the gate of \( M3 \) by an amplifier that forces \( V_{DS1} \) to be equal to \( V_C \). Therefore, the voltage variations at the drain of \( M3 \) affect \( V_{DS1} \) to a lesser extent because amplifiers regulate this voltage. With the smaller variations at \( V_{DS1} \), the current through \( M1 \) and hence output current remains more constant, yielding a higher output impedance.

\[ R_{OUT} = A_g m_{31} f_{o1} \]

It is one of solutions using regulated cascode to replace the auxiliary amplifier in order to overcome restrictions on Figure 1.2.(a). The circuit in Figure 1.2.(b) proposed in uses a single transistor, \( M5 \), to replace the amplifier in Figure 1.2.(a). This circuit called regulated cascode which is abbreviated to RGC. The RGC uses \( M5 \) to achieve the gain boosting by increasing the output impedance without adding more cascade devices.
Figure 1.2.(a). Basic triode transconductor structure

\[ V_{DS1} \] is calculated by follows: Assuming M5 is in saturation region in Figure 1.2.(b). It can be shown that:

\[ I_D = \frac{B}{2} (V_{GS} - V_T)^2 \]

Figure 1.2.(b). Simple RGC triode transconductor

GM can be tuned by using a controllable voltage source VC or current source IC. However, it is preferable in practice to use a controllable voltage source VC for lowering power consumption since \( V_{DS1} \) only varies as a square root function of IC. Simple RGC transconductor using a single transistor to achieve gain boosting can reduce area and power wasted by the auxiliary amplifiers. However, it still has some disadvantages. First, it will cause an excessively high supply-voltage requirement and also produce an additional parasitic pole at the source of transistors. Therefore, it can not apply to the low-supply voltage design. Second, the tuning range of \( V_{DS1} \) is restricted. The smallest value of \( V_{DS1} \) is when \( V_C = 0 \). In other words, \( V_{DS1} \) can not be set to zero. \( V_{DS1} \) is as low as possible and the best value is zero. Third, VT dependent GM may be a disadvantage due to the substrate noise and VT mismatch problems. Another RGC transconductor that can apply to the low-voltages applications. The circuit overcomes the disadvantages mentioned above is to utilize PMOS transistor that can operate in saturation region as gain boosting. The use of this PMOS gain boosting in the feedback path can result in a circuit with a wide transconductance tuning range even at the low supply voltage. At the maximum input voltage, M3 may be forced to enter triode region, especially if the dimension of M2 is not properly selected, resulting in a lower dynamic range.

Figure 1.2.(c) RGC transconductor with PMOS gain stage

1.3 Transconductor using adaptive biasing

The transconductor using adaptive biasing is shown in Figure 1.3. All transistors are assumed to be operated in saturation region, neglecting channel length modulation effect. First, transistor M3 is absent, and output current as a function of two input voltages \( V_{in1} \) and \( V_{in2} \) is obtained as

\[ I_{OUT} = I_{out1} - I_{out2} = \sqrt{\frac{B}{2} (V_{in1} - V_{in2})^2} \]

where \( I_{SS} \) is a tail current and equals \( I_B \). An adaptive biasing technique is using a tail current containing an input dependent quadratic component to cancel the nonlinear term.
Consequently, the circuit in Figure 1.3 changes the tail current by adding transistor M3. The tail current will be changed by

$$I_{SS} = I_B + I_C$$

where $I_B$ is tail current of differential pair and $I_C$ is the compensating tail current that cancel nonlinear term. Therefore, the transfer characteristic is changed by:

$$I_{OUT} = I_{out1} - I_{out2} = \frac{\beta}{4} V_{in1} - V_{in2}$$

where $\beta$ is transconductance of the differential pair.

2. Proposed Technique

Auxiliary degenerated MOS differential pair

This method uses auxiliary degenerated MOS differential pair to drive the bulk of the main degenerated MOS differential pair. Fig 5.1 depicts the schematic diagram of the transconductor of the supplementary linearization technique. The control signals are obtained and applied to the bulk terminal of the main pair. Same inputs are applied to main differential pair as well as auxiliary MOS differential pair. The main idea of using this approach is better linearity is obtained by feeding the bodies of the input transistors with an attenuated and inverted replica of the differential input voltage. By choosing proper attenuation factor, the linearity can be maximized. The transistor dimensions and current bias both of this auxiliary pair are been scaled down with the same ratio, $m = \frac{W_1}{L_1} = \frac{W_2}{L_2}$ compared to the dimensions and current bias of the main pair.

Thus, the dc source voltage of M1-M2 and M3-M4 are the same, while keeping in mind low area and bias current overhead. The degeneration resistor for auxiliary pair is implemented using a series of resistors $2R_1 + R_2$ which is equal to $mR_{DEG}$ according to the scaling adopted. The current equation of MOS in saturation is given by:

$$i_D = K \frac{W}{L} (V_{GS} - V_{TH} - \sqrt{2} \frac{v_{DS}}{v_{DS}})^2$$

The circuit operation depends on the body effect and we know that body effect results in increase in threshold voltage. Thus the threshold voltage is given by the expression:

$$V_{TH} = V_{TH0} + \gamma \sqrt{2} \frac{V_{DS}}{v_{DS}} - \sqrt{2} \frac{V_{DS}}{v_{DS}}$$

The total bulk source voltage of M1 and M2 is a small signal quantity, i.e., $V_{BS} = v_{BS}$ because no current flows through resistor string at dc.

$$i_D = K \frac{W}{L} [V_{GS} - V_{TH} - \gamma \sqrt{2} \frac{v_{DS}}{v_{DS}} - \sqrt{2} \frac{V_{DS}}{v_{DS}}]^2$$

Where $V_{GS}$ is the over-drive voltage stated as $V_{GS} = V_{TH} + \gamma \sqrt{2} \frac{V_{DS}}{v_{DS}}$ and the power series coefficients are:

$$n_1 = \gamma \left( \frac{2\gamma}{40\gamma} \right), n_2 = \gamma \left( \frac{3\gamma}{31\gamma} \right), \text{ and } n_3 = \gamma \left( \frac{2\gamma}{119\gamma} \right)$$

3. Conclusion

The effect of mobility reduction in a linear transconductor with input signal attenuation and resistive source degeneration is analyzed theoretically and it has been shown that the cubic non-linearity in the attenuating stage partially cancels out the distortion component in the source degenerated OTA. In this work a study of bulk
linearization in a differential pair to enhance its linear range has been presented. In bulk linearization is proposed for high speed OTAs with a reduced harmonic distortion.

4. References

[1] Joel Gak, Member, Matías R. Miguez, “Nanopower OTAs with Improved Linearity and Low Input Offset Using Bulk Degeneration” IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—2014


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