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Review Paper on Design of SAR-ADC Using Double Tail Comparator

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Abstract*: The demand for area efficient, ultra-low-power, and high rate analog to digital converter is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. Comparator is foremost block of ADC. In this paper conventional comparator is studied. Drawbacks of conventional comparator are overcome by a new design of proposed comparator. The proposed comparator enhances the speed of the ADC, It affects two important factors: first, it increases the initial output voltage difference at the beginning and second, it enhances the effective transconductace of the latch. The main motivation is to achieve high speed with medium resolution using capacitor array DAC in 90nm technology.*

1. Introduction

A conventional successive approximation analog to digital converter consists of a sample-and-hold (S/H) circuit, a comparator, a successive approximation register (SAR), and a digital-to-analog converter (DAC). Comparator block consumes more power compare to other blocks of ADC. In this paper novice approach of comparator is given. Tyro comparator works on low power, low voltage and gives high speed over reduced latch delay time. To design high speed comparator for low supply voltage is challenging task. Name of new comparator is double tail comparator; it includes some extra transistor in circuit. Double tail comparator does not require stacking of too many transistors or boosted voltage. The DAC present in SAR ADC is of different types such as, capacitor-based DAC, switched-current DAC or R-2R ladder DAC. Among these convertors the capacitor based DAC has become more popular. Because capacitor base DAC has zero quiescent current. double-tail circuitry is place between SAR-ADC in order to optimize the power performance and the circuit operates on high-speed. This overall modification result in considerable saving of power. The double-tail topology can operate faster and can be used in lower supply voltages, while consuming nearly the same power as the conventional dynamic comparator. Many high-speed ADC require high-speed, low power comparators with small chip area.

2. Review papers

Babayan-Mashhadi et.al In this paper, an analysis on the delay of the dynamic comparators is presented and analytical expressions are derived. This paper tells comparator is one of the fundamental building blocks in most analog-to-digital converters (ADCs). Many high speed ADCs, such as flash ADCs, require high-speed, low power comparators with small chip area. High-speed comparators in ultra-deep submicrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes. Hence, designing high-speed comparators is more challenging when the supply voltage is smaller. The conventional dynamic comparator is mostly used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption. The given circuitry has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. [1]

Stefano D'Amico et. Al In this paper, a low-power intrinsically matched 1-Gs/s 5-bit ADC is described. The comparator is the core circuit of an ADC. In fast ADCs, comparators based on latch-type sense amplifiers (SA) are widely used because of their ability to achieve fast decisions by means of a strong positive feedback. Comparator has been adopted, with two different biasing schemes. However, since in both cases the MOS transistor sizes remain the same, comparators have similar offset. Low power consumption is achieved by performing interpolation by using dynamic comparators. Intrinsic matching of devices has been ensured by using larger transistor sizes. The resulting higher kickback noise on comparators inputs has been mitigated by adopting an improved version of the dynamic comparator. [2]

Siddharth Chaudhari et.al analysis made about conventional comparator and proposed double tail comparator. Double tail comparator does not require supply voltage boosted technique or stacking of too many transistors. Latch delay time reduced by adding few transistors to the conventional double tail comparator. Now this reduced delay time also results in power saving. To compare proposed comparator with conventional comparator all circuits are simulated in 0.18um CMOS technology at VDD = 1.8 V. With this they get average power consumption for conventional comparator. Pre layout simulation results in 0.181um CMOS technology confirmed that the average power of modified comparator is reduced. [3]

Saurabh A. Malik et.al In this paper a new design of double tail comparator is proposed for high frequency of data conversion and is compared with the best available recently proposed double tail comparator design in term of area on chip power utilization, delay consideration and PDP. For a frequency higher than 350 MHz the power consumption is less for the proposed double tail comparator design, which keeps on getting better with every rising frequency. The maximum frequency of operation is also increased from 1.7 GHz to 2.5 GHz along with lesser delay which is significant considering the need of high speed devices. Apart from the proposed DT comparator shows an improvement of 23.57% in terms of area than the previous best design. [4]

Masaya Miyahara et.al developed low-offset latch comparator by using new offset cancellation technique. The developed comparator requires two phase such as reset mode and regeneration mode. The offset voltage of the comparator is caused by the mismatch of the transistor's threshold voltages. Therefore, due to input common mode variation increasing offset voltage can be suppressed by using the given methodology. The offset voltage cancellation or calibration techniques are vital for realizing a low voltage offset comparator. Conventional double-tail latched comparator had been designed by using conventional latched comparator. Each stage's contribution to the offset voltage of the conventional comparator obtained from Monte-Carlo simulation.[5]

Mehdi Saberi et.al In this paper, the structure of a binary-weighted capacitive digital-to-analog converter (DAC) in a successive approximation analog-to-digital converter (SA-ADC) is modified to a unary or segmented configuration to reduce the power consumption and improve the static linearity performance. It should be noted that not only the comparator noise (including the kickback noise), but also its nonlinear input capacitance affect the ADC performance.[6]

Sanyi khan et.al developed the technology to analyse the static input offset voltage in a dynamic comparator in the same way as in the traditional operational amplifier. In this paper author presented a novel balanced method to analyze input referred offset voltages in dynamic comparators. The method solves the problem that in a dynamic comparator the operating points of transistors are not well defined in the transient process. In this method, they first solve the bias point at comparison phase when the circuit is perfectly balanced without any mismatch. Second, very little emphasis is placed on mismatch of internal parasitic capacitance[7]

3. Problem Identification

The reference papers which are mentioned above have some drawbacks as these papers only focus on average power consumption. Analysis of comparator is presented in which dynamic comparator proposed with high speed in order to improve the performance of the dynamic comparator in terms of power. In above papers the common structure of conventional and double tail comparator is explained and compared the delay and power of those comparators. The delay of this comparator is comprised of two time delays, t0 and T1 latch. The delay t0 represents the capacitive discharge of the load capacitance CL until the first p-channel transistor turns on. The large number of signal types to be digitized has led to a diverse selection of data converters in terms of architectures, resolution, and sampling rates. In this comparator, both intermediate stage transistors are in cut-off, hence they do not play any role in improving the effective transconductance of the latch.

4. Praposed Work

In reference paper ADC is design were double tail comparator is main block. Double tail comparator is advantageous over other conventional comparators with respect to power consumption, transit speed, delay parameter and many more. Circuit diagram for double tail comparator is given in fig 1. Operation of double tail comparator is as fallows during reset phase (CLK = 0, Mtail1 and Mtail2 are off, avoiding static power), M3 and M4 pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground. During decision-making phase (CLK = VDD, Mtail1, andMtail2 are on), transistors M3 and M4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off(since fn and fp are about VDD). Thus, fn and fp start to drop\with different rates according to the input voltages. Suppose VINP > VINN, thus fn drops

faster than fp, (since M2 provides more current than M1). As long as fn continues falling, the corresponding pMOS control transistor (Mc1 in this case) starts to turn on, pulling fp node back to the VDD; so another control transistor (Mc2) remains off, allowing fn to be discharged completely.

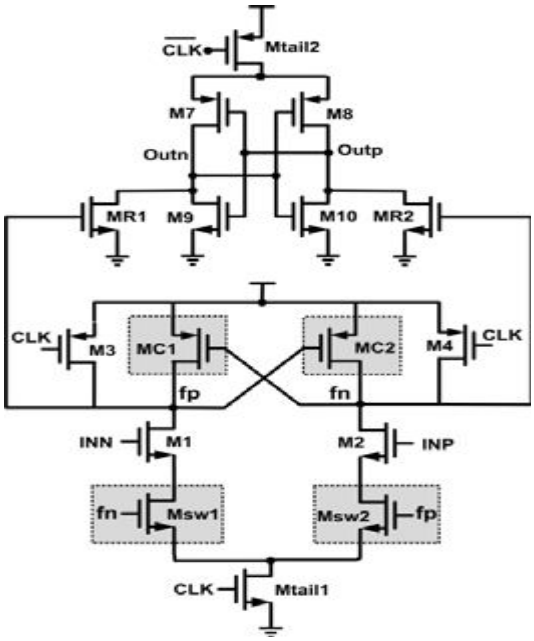


Figure1. Double Tail Comparator

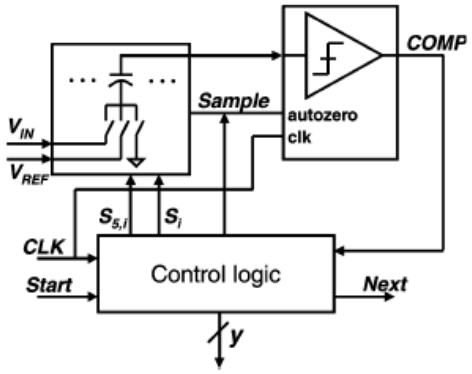


Figure 2. SAR logic block

The SAR architecture (Figure 2.) mainly uses the binary search algorithm. The SAR ADC consists of fewer blocks such as one comparator, one DAC (Digital to analog Converter) and one control logic. The main advantage of SAR ADC is good ratio of speed to power. The SAR ADC has compact design compare to flash ADC, which makes SAR ADC inexpensive. The physical limitation of SAR ADC is, it has one comparator throughout the entire conversation process. If there is any offset error in the comparator, it will reflect on the all conversion bits. The other source is gain error in DAC. However, the static parameter errors do not affect dynamic behavior of SAR ADC.

5. Module

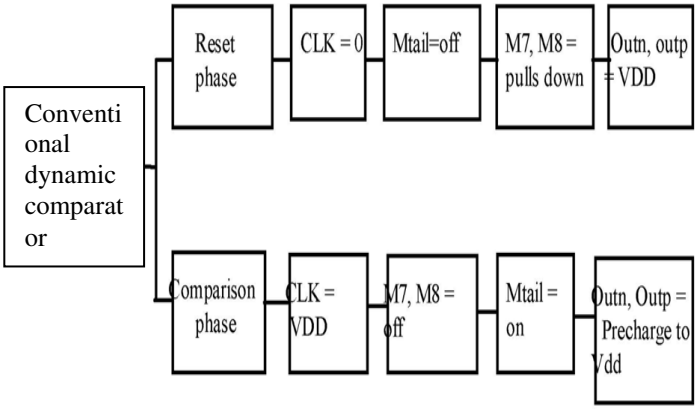


Figure 3: Working of the conventional dynamic comparator

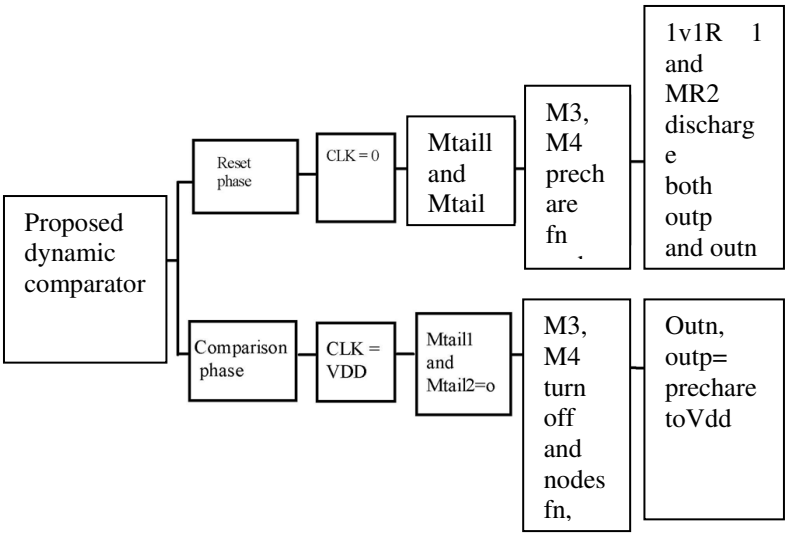
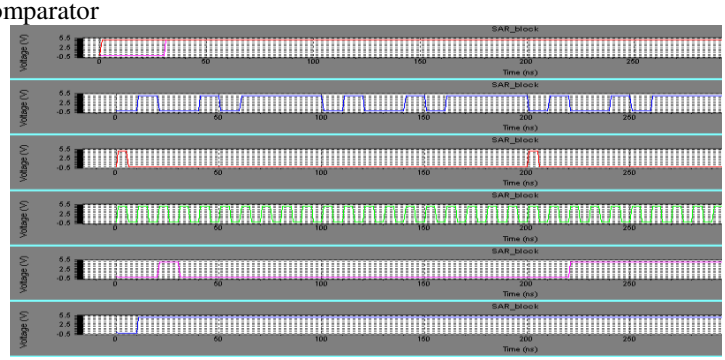


Figure 4. Working of the proposed double tail comparator



Output Waveform : SAR block output

6. CONCLUSION

We conclude that, the designing of SAR-ADC using UDSM CMOS technology is more efficient for the estimation and optimization of the power performance. A SAR ADC is suitable for medium resolution with higher speed. Furthermore, the SAR ADC has many applications such as wireless communication, and medical Instruments. Capacitor array DAC is better compare to resistor string DAC. Matching of Capacitor can be achieved better compare to resistor matching.

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