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Design of Low Delay Look Ahead Adder and Ripple Adder

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Abstract *: In recent years, a lot of attentions have been attracted by the reversible logic due to the characteristic of zero energy dissipation. In this paper, the author proposed a 16 bit carry look-ahead adder is constructed by four 4 digits groups based on the theory of reversible logic, which has the advantages of theoretical zero power dissipation and high efficiency. This paper focuses on the implementation 16 and bits of highly optimized area efficient Ripple carry adder (RCA) and Carry look ahead (CLA) adders. Ultimately, we can establish that the Carry look ahead adders are so greatest among all the formerly active designs. All these processes will be Simulated & Synthesized on the ISE Xilinx 14.7 software*

Keywords*: Reversible gates, Quantum Computer, Quantum cost, Quantum gates, two's complement*

I Introduction

The inevitability of achieving zero power dissipation in low power digital design yields the concern in the invention of Reversible logic gate which plays essential role in the modern computing. Reversible logic has received immense attention in the newsworthy years due to their capability to decrease the power indulgence which is the main constraint in low power VLSI design. It has wide applications in low power CMOS and Optical information processing, DNA computing, quantum computation and nanotechnology. Irreversible hardware computation results in energy dissipation due to information loss. According to Landauer's research, the amount of energy dissipated for every irreversible bit operation is at least KTln2 joules, where K=1.3806505*10-23m 2 kg-2K -1 (joule/Kelvin-1) is the Boltzmann's constant and T is the temperature at which operation is performed [1]. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works the heat dissipated by them will be so large that it affects the performance and Dissipate from a system as long as the system allows the Reproduction of the inputs from observed outputs [2].

Reversible logic supports the process of running the system both forward and backward. This means that reversible computations can generate inputs from outputs and can stop and go back to any point in the computation History. A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments, i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs Energy dissipation can be reduced or even eliminated if computation becomes Information-lossless

II Motivation behind Reversible Logic

High-performance chips releasing large amounts of heat impose practical limitation on how far can we improve the Performance of the system. Reversible circuits that conserve information, by uncomputing bits instead of throwing them away, will soon offer the only physically possible way to keep improving performance. Reversible computing will also lead to Improvement in energy efficiency. Energy efficiency will fundamentally affect the speed of circuits such as nano-circuits and therefore the speed of most computing applications. To increase the portability of devices again reversible computing is required. It will let circuit element sizes to reduce to atomic size limits and hence devices will become more portable. Although the hardware design costs incurred in near future may be high but the power cost and performance being more dominant than logic hardware cost in today's computing era, the need of reversible computing cannot be ignored

III Reversible Logic Gates

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-Out is not allowed as one–to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of

reversible circuit design, there are many parameters for determining the complexity and performance of circuits. The number of Reversible gates (N): The number of• reversible gates used in circuit. The number of constant inputs (CI): This refers to the• number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function. The number of garbage outputs (GO): This refers to the• number of unused outputs present in a reversible logic

III Ripple Adder

Ripple carry adder A ripple carry adder is a digital circuit that produces the arithmetic sum of two binary numbers.[4] may be capable of constructed with full adders connected in cascaded through the carry output beginning every full adder associated to the carry input of the next full adder in the chain the interconnection of four full adder (FA) circuits to provide a 4-bit ripple carry adder observe from so as to the input is beginning the accurate side because the first cell traditionally represents the least significant bit (LSB).

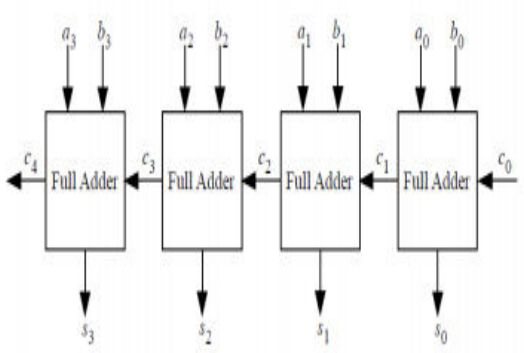

Fig. 1. 4-bit full adder.

IV Carry Look Ahead Adders

The enter to speed up adding up is influential the carry in to the soaring order bits sooner. There are a assortment of scheme to expect the carry so that the nastiest case scenario is a function of the log2 of the number of bits in the adder. These preventative signals are quicker since they go throughout fewer gates in succession, but it takes many more gates to anticipate the proper carry a key to understanding fast-carry schemes is to remember that, unlike soft ware, hardware executes in parallel whenever inputs change Look-Ahead Adder a Carry Look-Ahead adder (CLA) is a type of adder used to improve speed by reducing the amount of time required to determine carry bits. It can be contrasted through the simpler, but frequently slower, ripple carry adder intended for which the carry small piece is designed alongside the sum bit, and each bit must wait until the previous carry has been

V Literature Survey

Neelam Somani et.al 2016 Reversible logic has represented itself as a prominent technology which plays an important role in Quantum Computing. Theoretically Quantum Computers operates at high speed and consumes less power. Furthermore, Reversible logic can break the conventional speed of power trade-off. To prove this we are implementing Ripple Carry Adder and Carry Look Ahead Adder using reversible logic gates. The paperpresents efficient adder circuits using Peres gate, New fault Tolerant gate and Double Feyman gate. The complexity, simulated outputs and the speed parameters for the Adder Circuit have been indicate during the Quartus II 9.1 edition and Model-sim tool .Moreover, the quantum algorithms can potentially solve NP-complete problems. Furthermore, doing high performance functions beyond the limit of deterministic computer systems is possible by only reversible logic. Quantum operations are unitary in nature which is reversible and hence the arithmetic operations like adders can be implemented using the reversible logic.

Omid Akbari1, Mehdi Kamal1,2et.al. 2016 In this paper, we propose a fast yet energy-efficient configurable approximate carry look-ahead adder (RAP-CLA). This adder has the ability of switching between the approximate and exact operating modes making it suitable for both error silent and exact applications. The structure, which is more are a and power efficient than state-of-the-art reconfigurable approximate adders, is achieved by some modifications to the conventional carry look ahead adder (CLA). The efficacy of the proposed RAP-CLA adder is evaluated by comparing its characteristics to those of two state-of-the-art reconfigurable approximate adders as well as the conventional (exact) CLA in a 15nm Fin FET technology. The results reveal that, in the approximate operating mode, the proposed 32-bit adder provides up to 55% and 28% delay and power reductions compared to those of the exact CLA, respectively, at the cost of up to 35.16% error rate. It also provides up to 49% and 19% lower delay and power consumption, respectively, compared to other approximate adders considered in this work. Finally, the effectiveness of the proposed adder on two image processing applications of smoothing and sharpening is demonstrated. The study shows that, on average, PSNR reductions of 12% and 16%, respectively, may be achieved by employing the proposed adder.

Christopher L. Ayala, Member, IEEE 2016 Superconductor-based adiabatic quantum-flux parameter on (AQFP) logic holds tremendous promise towards building extremely energy efficient computing systems with bit energies approaching 100 $k\ B\ T$. The majority logic gate is the basis for how all AQFP logic gates are created. By reconsidering the logic design approach of digital

circuits using majority logic instead of conventional AND/OR/NOT logic, circuits can potentially use fewer gates overall. This may lead to lower circuit complexities in terms of Josephson junctions, and in turn lower power consumption as well as lower latencies. As a first step towards exploiting majority logic in AQFP technology, we explore how majority-logic-optimized designs of the Kogge-Stone and Brent-Kung adder architectures scale in terms of complexity, latency, area and energy/operation as we increase the data word size from 8-bit to 64-bit. Next, we implement 8-bit prototypes of both adders for experimental demonstration. The designs have been fabricated using the 2.5kA/cm2 AIST standard process 2and have demonstrated

successful operation in low-frequency testing. Both adders consist of ~1000 Josephson junctions and are designed for 5 GHz operation with a 5 cycle latency

In 2012, R.LANDAUER portrayed that the sensible irreversibility is connected with physical irreversibility and requires a negligible warmth era for each machine cycle. For irreversible logic calculations, every piece of data lost produces kTlog2 joules of heat energy, where k is Boltzmann's steady and T the supreme temperature at which calculation is performed. In customary framework the great many gates used to perform consistent operations. Creator demonstrated that heat dissipation avoidable if framework made reversible [1]. Calculated to begin calculating its own result and carry bits

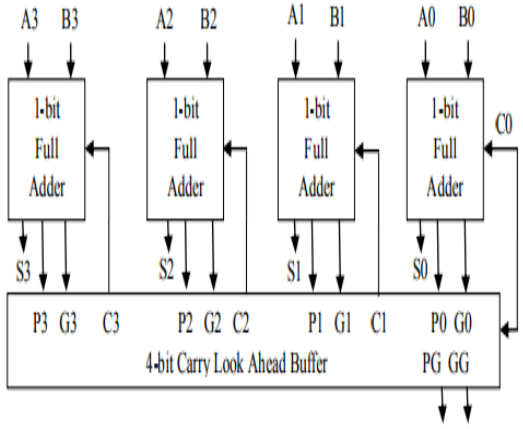

Fig.2 Carry Look-Ahead Adder

In 2015, c.h.bennett depicted that if a calculation is done in Reversible rationale zero vitality dissemination is conceivable, as the measure of vitality scattered in a framework is specifically identified with the quantity of bits eradicated amid calculation. The outline that does not bring about data misfortune is irreversible. Arrangements of reversible gates are expected to plan reversible circuit. Reversible gate can produce remarkable output vector from every input vector and the other way around [2].

In 2008, Majid Mohammdi et.al exhibited those quantum gates to execute the parallel reversible rationale gates. Quantum gates V and V+ to be spoken to in truth table structures. Creator demonstrated that few reversible circuit benchmarks are enhanced and contrast and existing work. Another behavioral model to speak to the V and V+ quantum gates based on their properties. This model used to recreate the quantum realization of reversible circuits [3].

In 2010, D.Michael Mill operator and Zahra Sasanian exhibited the lessening the quantity of quantum gate expense of reversible circuits. To diminish the quantum cost enhances the proficiency of the circuit. To decide a quantum circuit is to first union circuits made out of parallel reversible gates then guide that circuit to a proportional quantum gate acknowledgment [4] CMOS, Quantum PC, Nanotechnology, Optical registering and self-repair [5].

In 2011, Md.Mazder Rahman et.al displayed a quantum gate library that comprises of all conceivable two-Qubit Quantum gates which don't produce trapped states. These gates areutilized to decrease the quantum cost of reversible circuits. They proposed a two-qubit quantum entryway library that assumes a noteworthy part in decreasing the quantum expense of reversible gates [6]. **In 2012, B.Raghu Kanth et.**al depicted that actualizing of reversible circuit reducing garbage outputs, gate count and constant inputs, gates tally and consistent inputs. Expansion, Subtractions operations are acknowledged utilizing reversible DKG gate and it contrast and ordinary doors. The proposed reversible adder/subtractor
circuit can be connected to outline of complex frameworks in nanotechnology [7].

In 2012, Mr. Devendra Goyal exhibited VHDL CODE of all Reversible Rationale Entryway, which give us to plan VHDL CODE of any complex successive circuit. Here creator have been attempted to make the VHDL code however much as could reasonably be expected. Creator can reenact and combination it utilizing Xilinx programming [8].

In 2013, Marek Szyprowski exhibited a device for minimizing the quantum cost in 4-bit reversible circuits. Here Creator demonstrated that for benchmarks and for plans taken from late distributions it is conceivable to acquire sparing in quantum cost contrasting and existing circuits [9].

In 2013, Raghava Garipelly gave that the essential reversible logic gates, which in planning of more intricate framework having reversible circuits as a primitive segment and this can execute more convoluted operations utilizing quantum computers.

Creator presented some new gates which are BSCL, SBV, NCG, and PTR and so forth [10].

In 2014, Ashima Malhotra et.al portrayed that reversible adjusted Fredkin entryway used to plan the multiplexers with low quantum cost and contrast it and existing work. They likewise look at the quantum expense of multiplexers outline utilizing, Fredkin door with Changed Fredkin gate used to plan the multiplexers [11]

VI Conclusion

We have presented an approach to the realize the multipurpose binary reversible gates. Such gates can be used in regular circuits realizing Boolean functions. In the same way it is possible to construct multiple-valued reversible gates having similar properties. The proposed asynchronous designs have the applications in digital circuits like a Timer/Counter, building reversible ALU, reversible processor etc. This work forms an important move in building large and complex reversible sequential circuits

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