

Design of 6-Bit TIQ Based CMOS Flash ADC for SOC Application

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Abstract: This paper presents 6-bit TIQ based CMOS Flash analog to digital converter using Rom encoder based on 180nm technology. The designed circuit mainly consists of Sample and Hold Circuit, TIQ Comparator, 1 out of N code generator, Rom based Encoder. Rom encoder is fastest when compared to Fat-Tree and Wallace tree encoder in terms of Speed in order to convert Thermometer code to Binary code. The power supply voltage used is 1.8 V for overall system. The sampling Frequency used is 100Ms/s. The simulation results includes average power consumption of 9.48m W. The results are obtained using Cadence virtuoso 180nm Technology.

1. Introduction

The real-world signals are analog in nature for example light, sound, video etc. To achieve digital signal, we need to convert the analog signal into digital form by using a circuit called analog-to-digital converter. Whenever the analog signal is needed back, digital-to-analog converter is required. As size of the transistor is scaled down to 0.065 μ m in 2007 according to semiconductor roadmap system on chip has demands in wireless application and also in broadband, consumer electronics like DVD, digital cameras, videogames and military application. System integrates all electronic components in to single integrated circuits which contains functions of analog, digital and mixed signal circuits on single chip solution, which helps in reduction in chip silicon area, size of board and packaging costs. A high-speed A/D converter is an essential part of SOC products.

1. SAMPLE AND HOLD CIRCUIT

The sample-and-hold(S/H) circuit main function is to sample the analog input signal and hold these samples taken at uniform intervals over a period of time such that sampling rate or clock rate can be measured. The S/H circuit operation mainly involves two modes sample mode (acquisition mode) and the hold mode, whose durations are not equal. Output of the circuit is equal to the previously sampled input value in case of hold mode. In case of sample mode, output either tracks the input or it can be reset for some fixed value hence the circuit is often called as

track-and-hold(T/H) circuit. When the input CLK=1, the nmos1 is on and the S/H circuit samples the voltage of IN. When the CLK=0, the nmos2 is close and the S/H circuit holds the voltage sampled at CLK=1. In order to address the signal-dependent charge injection from nmos onto Vi, one more nmos2 was added and sized to have one-half the W/L of nmos1.

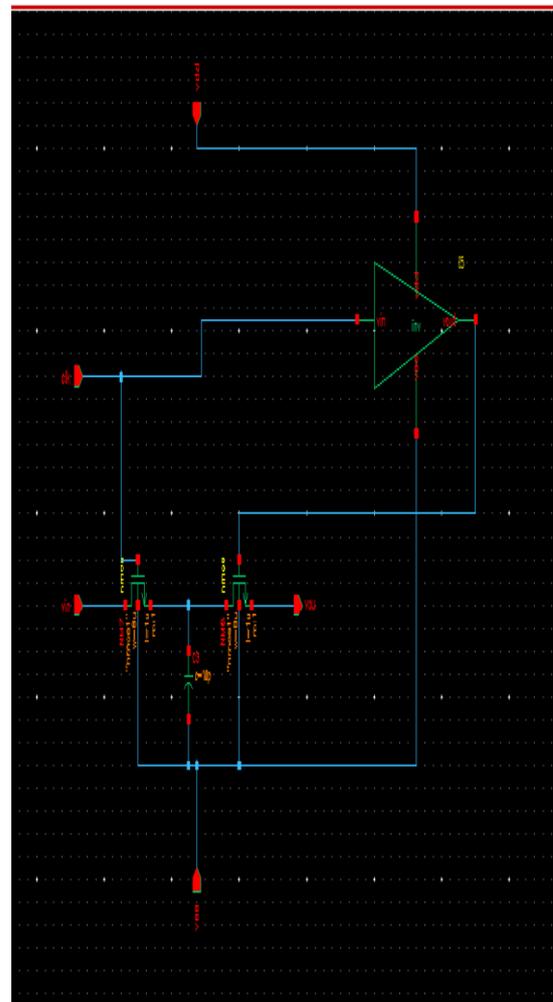


Figure 1 Schematic of Sample and Hold Circuit.

2. FLASH ADC

When compared to other ADC architectures, the Flash ADC is known for its fastest speed. The flash

ADC is known as the parallel ADC because of its parallel architecture. The results of conversion are available at the end of one clock cycle. Due to the parallel design, it is the fastest ADC among all the other types and is appropriate for large bandwidth applications such as radar processing data acquisition, high density disk drives, satellite communications, data communications and real-time oscilloscopes. It is also highly used in other types of ADCs such as pipeline ADCs and multi bit sigma delta ADCs.

Flash ADC is limited to a resolution of six to eight bits because the number of comparators utilized in these ADC are doubled if the resolution is enhanced by one bit. As the resolution increases it consumes a lot of power and becomes costly. Figure 3.7 shows the generic Flash ADC block diagram.

For a N bit ADC $2^N - 1$ comparator is needed. Each comparator is connected with one input to an analog input and another to a reference voltage. The reference voltage for the comparator is generated with the help of a resistor ladder.

The resistor ladder consists of $2N$ resistors. The reference voltages are uniformly spaced by least significant voltage between the smallest reference voltage and largest reference voltage. When the input voltage is less than the reference voltage of comparator it produces logic low otherwise, the comparator output is logic high.

The outputs of the comparators are coming in a special fashion known as thermometer code. It's named because it is like a mercury thermometer, where the mercury column always rises to the suitable temperature and no mercury is available beyond that temperature. Further this code is translated into a binary data with the assist of a thermometer to binary code converter.

Flash ADC requires huge number of comparators when the resolution increases. For example, a 6-bit flash ADC requires 63 comparators, but 1023 comparators are required for a 10-bit Flash ADC. This exponential increase of comparators needs a large die size which leads to huge amount of power consumption.

3. TIQ COMPARATOR

In ADCs, the comparator plays a main role on overall performance. Comparators is especially designed for open loop configuration without any feedback. Speed, Gain, power dissipation, offset and resolution are the important parameters of any type of comparators.

Comparators find application in peak detectors, zero crossing detectors, BLDC operating motors, switching power regulators.

Comparator main aim is to compare the input signal (V_{in}) with a reference signal (V_{reF}) and produce an output logic high or logic low depending on whether

the input signal is greater or lesser than the reference signal.

If $V_{in} > V_{ref}$ $V_{out} = \text{Logic High}$;

If $V_{in} < V_{ref}$ $V_{out} = \text{Logic Low}$;

TIQ comparator comprises of two cascaded inverters. Advantage of low power consumption of CMOS inverter and considerable higher speed achieved here. The comparator is the most important component in the ADC architecture.

Comparator main role is to compare the reference voltage with the input voltage (V_{in}) and produce output either logic '1' or logic '0'. If input voltage V_{in} is greater than reference voltage the output of comparator is '1' else '0'.

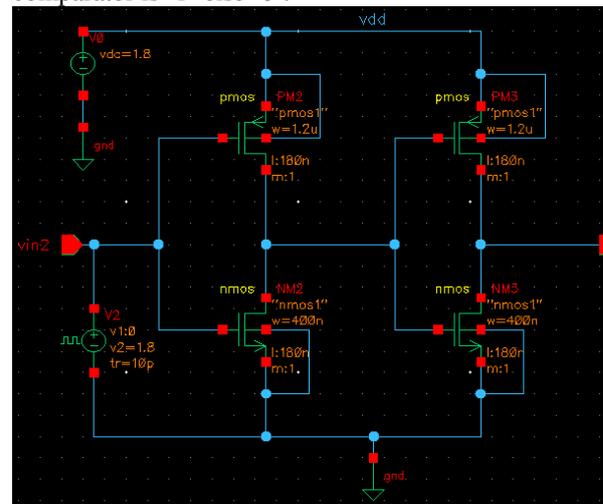


Figure 2 Schematic TIQ Comparator

Some of the advantages of using TIQ are:

- voltage comparator circuit is very simple.
- voltage comparison speed is very fast.
- resistor ladder circuit is eliminated.
- For comparison of voltages it doesn't require any switches, coupling capacitors or clock signals.
- TIQ comparator highly suitable for system on chip application as it is compatible with CMOS.
- Between the power supply rails only two transistors are present.
- Below $0.1\mu\text{m}$ feature size and 1.0 V power supply voltage, the TIQ comparator realization is possible with the advanced CMOS technology.

4. Threshold Voltage of comparator

Mathematically the threshold voltage of inverter (V_m) is defined at point where $V_{in} = V_{out}$

$$V_m = \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}}(V_{DD} - |V_{TP}|) + V_{TN}}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}} \quad (1)$$

Where V_{tn} is threshold voltage of NMOS and V_{tp} represent the threshold Voltages of PMOS respectively, $W_p = P_{mos}$ width, $W_n = N_{mos}$ width, $V_{DD} =$ supply voltage, $\mu_n =$ electron mobility, $\mu_p =$ hole mobility. Assuming both length of Pmos and Nmos are equal. At the First inverter, the analog input signal quantization set by V_m depending on W/L ratios of PMOS and NMOS. The stage two is used to increase the Voltage Gain.

5.1 out of N Code

Once the comparator produces the output as the thermometer code, thermometer code is converted as binary code using thermometer to binary encoder. Thermometer to binary encoder generally converts it to a binary code (BC) in two steps. The TC is converted to the 1 out of n code using XOR logic then this code is converted to binary code.

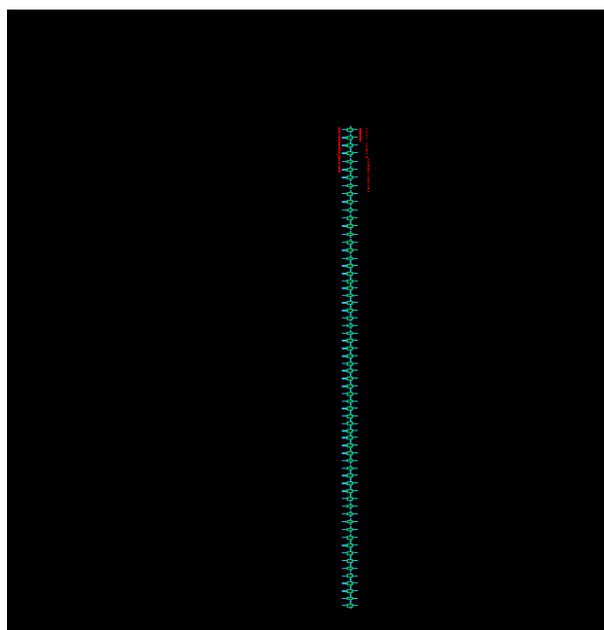


Figure 3 Schematic 1 out of N Encoder

6. Rom Encoder

In order to convert 1-out of -n code to a BC, a Rom type can be used. NOR ROM circuit is optimized with respect to transistor sizes is mainly developed for high speed conversion. The ROM based method is having two stages. In the initial stage, the thermometer code is translated in to 1 out of 2^{N-1} code. This can be made by using array of NAND gates. The second stage is the ROM configuration which receives the 1 out of 2^{N-1} code as input and chooses suitable row in the ROM and generates the binary output. In TIQ flash ADC, the speed of ROM is the predominant factor because signal delay of

ROM is algorithmically $O(N)$. where N is the number of ROM inputs.

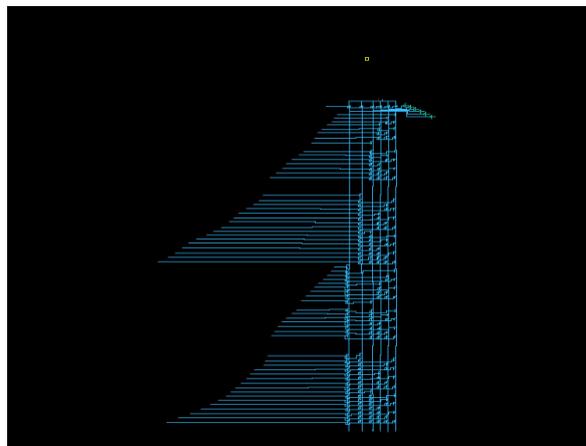


Figure 4 Schematic ROM Encoder

7. Proposed Flash ADC

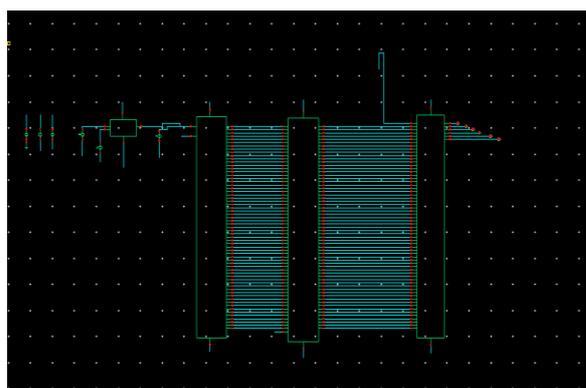


Figure 5 Design Under Test



Figure 6 Sample and Hold output

The table shows the summary of proposed system

| | |
|-----------------|--------|
| Technology(nm) | 180nm |
| Supply voltage | 1.8v |
| Input Frequency | 100MHz |
| Number of Bits | 6 |

| | |
|---------------|---------|
| Average power | 9.48mW |
| SNR | 37.88dB |

TABLE I SUMMARY OF PROPOSED SYSTEM

8. Acknowledgements

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9. CONCLUSION

In the proposed ROM Encoder based 6-bit Flash ADC structure, the simulation is done with the help of GPDK 180nm technology in CADENCE. In the proposed architecture, the main advantage is that the static power consumption is very low due to the absence of resistor bank. The average power consumption is 9.48mW for input frequency 100Mhz. In Future work, we can configure the layout part and we can find out area of the chip. By reducing the area of the chip by scaling down the MOS transistor we can reduce the cost of chip.

10. References

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