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Low Power and High Speed ALU using FinFET Technology

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Abstract: *FinFET is a new device structure of vertical double gate and become the alternative device for the nanoscale design. In this paper, A One-Bit ALU is designed and simulated in 32nm technology using FinFET device technology. Simulation results indicate that the proposed technique provides improvement in Average Power Consumption and the use of FinFET device increases performance speed of the device logic.*

Keywords: *FinFET, ALU, MosFET, Adder*

1. Introduction

As nanometer process technologies have advanced, chip density and operating frequency have increased, making power consumption in battery-operated portable devices a major concern. Even for no portable devices, power consumption is important because of the increased packaging and cooling costs as well as potential reliability problems. Thus, the main design goal for VLSI (very-large-scale integration) designers is to meet performance requirements within a power budget. [3] Therefore, power efficiency has assumed increased importance. This project explores how circuits based on FinFETs (fin-type field-effect transistors), an emerging transistor technology that is likely to supplement or supplant bulk CMOS) at 32-nm and beyond, offer interesting delay–power tradeoffs [7].

The desire to optimize the design metrics of performance, power, area, cost, and time to market (opportunity cost) has not changed since the inception of the IC industry. In fact, Moore's Law is all about optimizing those parameters. However, as scaling of manufacturing nodes progressed towards 20-nm, some of the device parameters could not be scaled any further, especially the power supply voltage, the dominant factor in determining dynamic power. [8] And optimizing for one variable such as performance automatically translated into big compromises in other areas, like power. Another limitation as processes approached 20-nm was the fact that lithography was stuck at ArF illumination source with a wavelength of 193nm while the process-critical feature was pushing sub-20nm. Optical innovations such as immersion lithography and double- atterning made that possible, but at the cost of increased variability. [9] There were also other innovations along the way such as High-K metal gate that alleviated – to a limited extent – gate leakage problems. But the fact remained that the design window for optimizing among the aforementioned design variables was shrinking [1]. Designing in FinFET broadens the design window once again. [4] Operating voltage continues to scale down, significantly saving on dynamic and static power. Short channel effects are reduced significantly, reducing the guard-banding needed to deal with variability. [10] And performance continues to improve compared too planar at an identical node. In fact, at very low power supply voltages, the performance advantage of the FinFET compared to its planar equivalent widens due to the superior gate control of the channel in the FinFET. [5] For memory designers, an added advantage of FinFETs is the significantly lower retention voltage requirements of FinFET-based SRAMs compared to planar FETs. Given the emerging metric of performance per unit power (Koomey's Law), one major design optimization benefit of FinFET compared too planar is much higher performance at the same power budget, or equal performance at a much lower power budget. This essentially gives designers the ability to extract the highest performance for the lowest power, a critical optimization for battery-powered devices. [3] One feature that makes the transition from designing with planar FETs to designing with FinFETs a little less complex is the fact that the back-end of the process is essentially the same, and therefore the part of the design flow associated with the physical implementation remains intact.

Scaling down the dimensions of MOSFETs is a continuous trend. The difficulties with reducing the size of the MOSFET include the semiconductor device fabrication process, the need for very low voltages, and with poorer electrical performance the necessity of circuit redesign and innovation [2]. It has been stated that smaller transistors switch faster, which is the main motivation for scaling down the dimensions of semiconductor devices [2].

2. FinFET Technology

FinFET in classified as a type of magnitude metal oxide semiconductor field affect transistor/MOSFET. It was first developed at the

university of Berkley California by Chenning Hu and his colleagues

In FinFET the NMOS in CMOS technology is replaced with N-FinFET and PMOS with P-FinFET, then, both gates of FinFET are tied together. [7] By using this approach, we can design a FinFET version of a CMOS logic circuit or a pass transistor logic circuit that retains the same functionalities as the MOSFET version. [6] In the meantime, FinFET provides better circuit performances and reduces leakage current through effective suppression of short-channel effect and near-ideal sub-threshold swing [9].

In the single-gate mode, the short channel effects (threshold voltage roll- off, sub threshold swing degradation and drain induced barrier lowering) are actually less severe than those of the device in the double-gate mode [2].

3. ALU

ALU is known as heart of any processor or controller and is a most vital part of the system. It generally performs basic arithmetic and logical operations. The efficiency, speed and power consumption of a processor largely depends on the ALU. The demand for a high speed processing has been increasing as a result of expanding computer calculations and signal processing applications. Higher throughput efficiency arithmetic operations are important to achieve the desired performance in many real-time signal analysis and image processing application.

4. Proposed ALU Design using FinFETs

The ALU which is to be implemented performs arithmetic operations such as addition and logical operations such as AND & OR. It is basically a three function ALU.

The ALU consists of NAND, NOR, Inverter, Full Adder and a 4:1 Mux. It performs three functions depending on the values of select lines, S0 and S1.

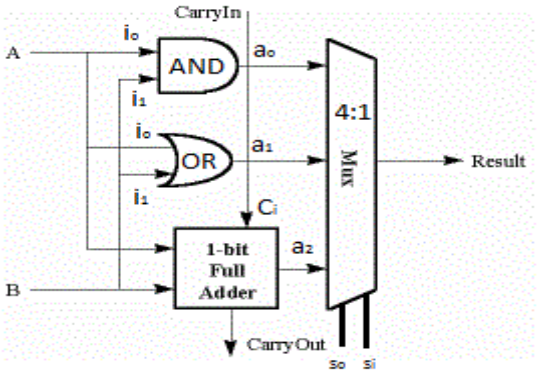


Figure 1: ALU Block Diagram

The logic circuits of AND, OR, Inverter, Full Adder and Multiplexer are made using CMOS logic, replacing the conventional MOSFETs with FinFETs.

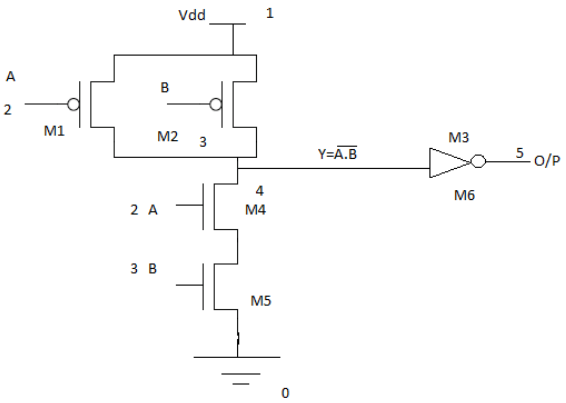


Figure 2: AND Gate

Figure 1 shows the block diagram of ALU, and the CMOS circuits with nodes naming of AND, OR and Full Adder are shown in Figure 2, 3 and 4 respectively.

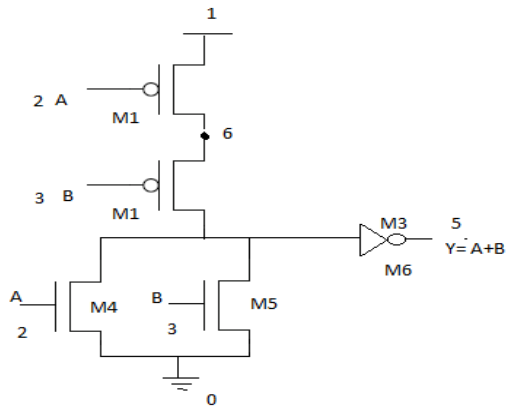


Figure 2: OR Gate

The transistor symbols used in the figure are of MosFET, FinFET symbols as studied in [3] is shown in figure 5. All the circuits are made in short gate configuration of FinFETs as shown in Figure 5.

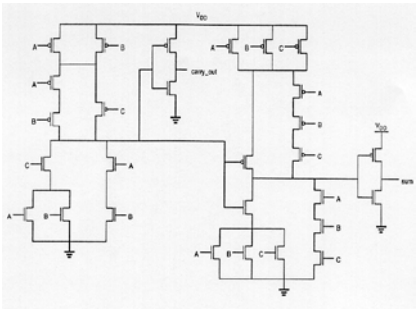


Figure 4: Full Adder

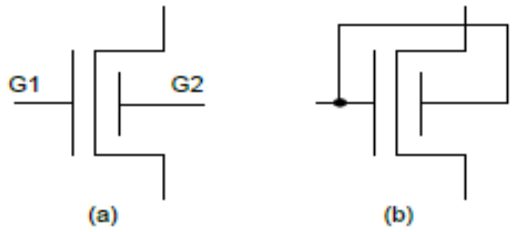


Figure 5: FinFET Configurations (a) Independent Gates (b) Shorted Gates [9]

The results are calculated on synopsis HSPICE by coding the nodes of the circuit diagram, the circuit diagram nodes are given different node name, for which the FINFET model from BSIMCMG is included and simulated. The 2-bit opcode selects the result of either logical or arithmetic block which will be the output of the ALU.

5. Simulation Results

The simulations performed in HSPICE are analyzed in this section. The table 1, 2 and 3 respectively show the Average power comparison in AND, OR and Full Adder respectively.

Table 1: Average Power AND Gate

	AND MOSFET(nW)	AND FINFET(nW)
Average Power	387	65.1

Table 2: Average Power OR Gate

	OR MOSFET(nW)	OR FINFET(nW)
Average Power	322	51.67

Table 3: Average Power Full Adder

	Full Adder MOSFET(nW)	Full Adder FINFET(nW)
Average Power	692	143

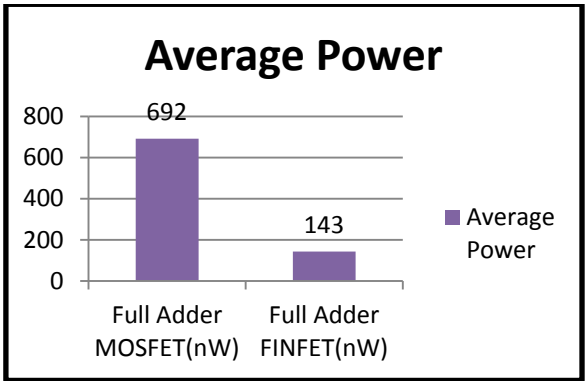


Figure 6: AND Gate Average Power

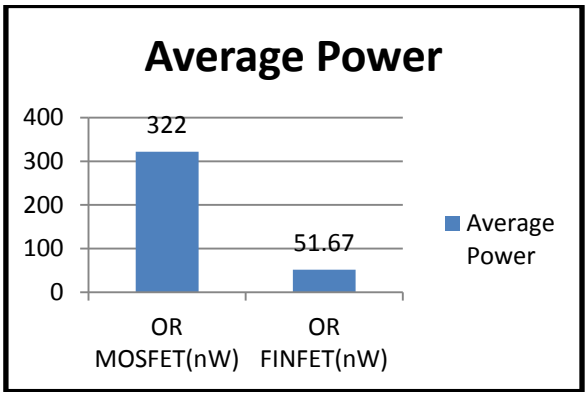


Figure 7: OR Gate Average Power

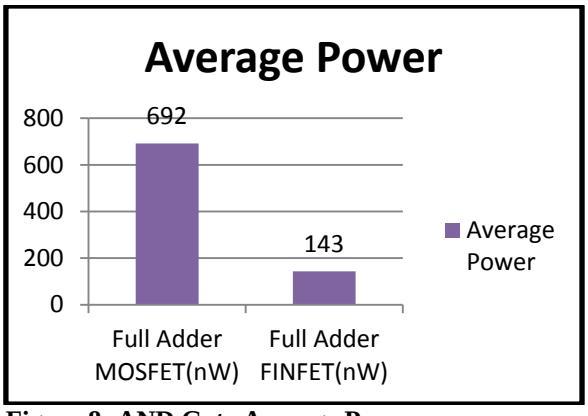
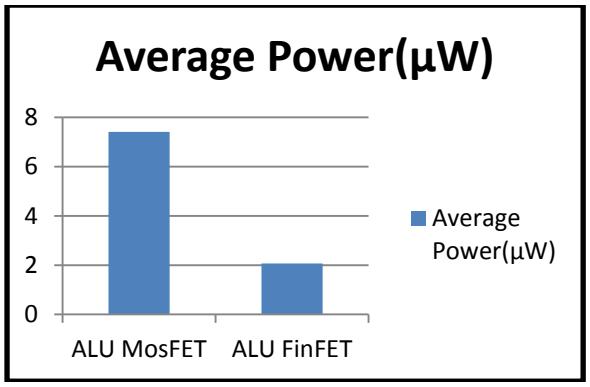


Figure 8: AND Gate Average Power

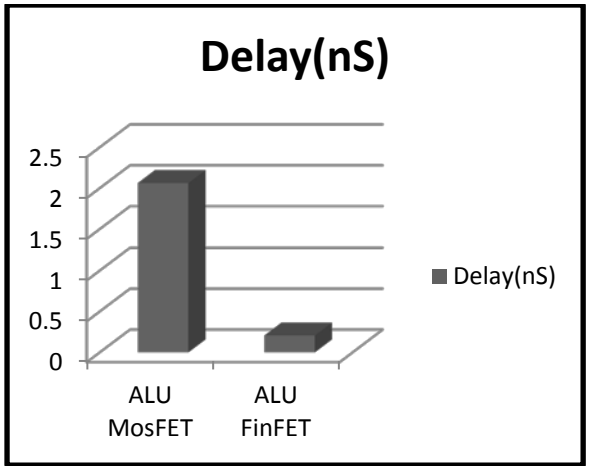
Figure 6, 7 and 8 are representing bar graphical representation of Average power consumption comparison in FinFET device circuit and MosFET device circuit. The results clearly prove that a lot of power saving and high efficiency can be achieved by the use of FinFET.

Figure 8: Average Power Consumption in ALU FinFET and ALU MosFET



The Figure 9 and 10 shows overall comparison of FinFET based ALU with MosFET based ALU. The model files of FinFET and MosFET are taken in 32nm technology from predictive technology models.

Figure 9: Delay in ALU FinFET and ALU MosFET



6. Conclusion

The use of FinFET over MOSFET in the proposed technique reduces average power consumption and delay in one bit ALU. The reduced short channel effects in FinFET and better control over the gate of the FinFET improves the average power delay in proposed technique. As already shown in simulation results, the Average Power Consumption and delay are greatly reduced in FinFET than MosFET. The MOSFET has been used widely in current technology. But below 32nm technology, controlling the channel of the MOSFET becomes difficult. So there is need to invent new technology which will allow us to design devices below 32nm technology.

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