A Brief Review on Characteristics of Static Random Access Memory

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Abstract— The power consumption is a main concern these days for long operational life. Although numerous types of techniques to decrease the power dissipation has been developed. One of the most adopted method is to lower the supply voltage. In this paper static random access memory parameters like low power, high performance circuit and characteristics and applications.

Keywords— SRAM, DRAM, CMOS

I. INTRODUCTION
Static random access memory (SRAM) is a type of semiconductor memory where the word static indicates that, unlike dynamic RAM (DRAM), it does not need to be periodically refreshed, as SRAM uses bistable latching circuitry to store each bit. SRAM exhibits data remanence, but is still volatile in the conventional sense that data is eventually lost when the memory is not powered.

For nearly 40 years CMOS devices have been scaled down in order to achieve higher speed, performance and lower power consumption. Due to their higher speed SRAM based Cache memories and System-on-chips are commonly used. Due to device scaling there are several design challenges for nanometer SRAM design.

Now we are working with very low threshold voltage and ultra-thin gate oxide due to which leakage energy consumption is getting increased. Besides this data stability during read and write operation is also getting affected. Intrinsic parameter fluctuation like random dopant fluctuation, line edge roughness and oxide thickness fluctuation further degrades the stability of SRAM cell. In order to obtain higher noise margin along with better performance new SRAM cells have been introduced. In most of these cell read and write operation are isolated to obtain higher noise margin. In this paper a comparative analysis of different SRAM cell at various technologies node has been carried out.

II. DIFFERENCE BETWEEN STATIC RAM AND DYNAMIC RAM?

Dynamic RAM is the most common type of memory in use today. Inside a dynamic RAM chip, each memory cell holds one bit of information and is made up of two parts: a transistor and a capacitor. These are, of course, extremely small transistors and capacitors so that millions of them can fit on a single memory chip. The capacitor holds the bit of information 0 or a 1. The transistor acts as a switch that lets the control circuitry on the memory chip read the capacitor or change its state.

Dynamic RAM has to be dynamically refreshed all of the time or it forgets what it is holding. The downside of all of this refreshing is that it takes time and slows down the memory. Static RAM uses a completely different technology. In static RAM, a form of flip-flop holds each bit of memory. A flip-flop for a memory cell takes 4 or 6 transistors along with some wiring, but never has to be refreshed. This makes static RAM significantly faster than dynamic RAM. However, because it has more parts, a static memory cell takes a lot more space on a chip than a dynamic memory cell. Therefore you get less memory per chip, and that makes static RAM a lot more expensive.

So static RAM is fast and expensive, and dynamic RAM is less expensive and slower. Therefore static RAM is used to create the CPU's speed-sensitive...
cache, while dynamic RAM forms the larger system RAM space.

III. TYPES OF SRAM

- Non-volatile SRAM
  Non-volatile SRAMs have standard SRAM functionality, but they save the data when the power supply is lost, ensuring preservation of critical information. SRAMs are used in a wide range of situations — networking, aerospace, and medical, among many others — where the preservation of data is critical and where batteries are impractical.

- Asynchronous SRAM
  Asynchronous SRAM are available from 4 Kb to 32 Mb. The fast access time of SRAM makes asynchronous SRAM appropriate as main memory for small cache-less embedded processors used in everything from industrial electronics and measurement systems to hard disks and networking equipment, among many other applications. They are used in various applications like switches and routers, IP-Phones, IC-Testers, DSLAM Cards, to Automotive Electronics.

  By transistor type
  Bipolar junction transistor — very fast but consumes a lot of power
  MOSFET — low power and very common today.

  By function
  Asynchronous — independent of clock frequency; data in and data out are controlled by address transition
  Synchronous — all timings are initiated by the clock edge(s). Address, data in and other control signals are associated with the clock signals

  By feature
  ZBT (zero bus turnaround) — the turnaround is the number of clock cycles it takes to change access to the SRAM from write to read and vice versa. The turnaround for ZBT SRAMs or the latency between read and write cycle is zero.
  Sync Burst (synchronous-burst SRAM) — features synchronous burst write access to the SRAM to increase write operation to the SRAM.

IV. CHARACTERISTICS OF SRAM

- SRAM is more expensive, but faster and significantly less power hungry (especially idle) than DRAM.
- It is therefore used where either bandwidth or low power, or both, are principal considerations.
- SRAM is also easier to control (interface to) and generally more truly random access than modern types of DRAM.
- Due to a more complex internal structure, SRAM is less dense than DRAM and is therefore not used for high-capacity, low-cost applications such as the main memory in personal computers.
- Clock rate and power :- The power consumption of SRAM varies widely depending on how frequently it is accessed; it can be as power-hungry as dynamic RAM, when used at high frequencies, and some ICs can consume many watts at full bandwidth. On the other hand, static RAM used at a somewhat slower pace, such as in applications with moderately clocked microprocessors, draw very little power and can have a nearly negligible power consumption when sitting idle — in the region of a few micro-watts.
- DDR SRAM — Synchronous, single read/write port, double data rate IO
- Quad Data Rate SRAM — Synchronous, separate read & write ports, quadruple data rate IO.

V. PARAMETERS

Noise margin
In electrical engineering, noise margin is the amount by which a signal exceeds the minimum amount for proper operation. It is commonly used in at least two contexts:

- In communications system engineering, noise margin is the ratio by which the signal exceeds the minimum acceptable amount. It is normally measured in decibels.
- In a digital circuit, the noise margin is the amount by which the signal exceeds the threshold for a proper '0' or '1'. For example, a digital circuit might be designed to swing between 0.0 and 1.2 volts, with anything below 0.2 volts considered a '0', and anything above 1.0 volts considered a '1'. Then the noise margin for a '0' would be the amount that a signal is below 0.2 volts, and the noise margin for a '1' would be the amount by which a signal exceeds 1.0 volt. In this case noise margins are measured as an absolute voltage, not a ratio. Noise margins for CMOS chips is usually much greater than TTL because the \( V_{OH_{min}} \) is closer to the power supply voltage and \( V_{OL_{max}} \) is closer to zero.

Noise margins are generally defined so that positive values ensure proper operation, and negative margins result in compromised operation, or perhaps outright failure.
Read Noise margin
It is the noise margin while reading.

Write Noise margin
It is the noise margin while writing.

Static noise margin
- Static noise is the DC disturbance present in logic gates.
- The worst case occurs when the static noise is adversely present in all logic gates in the same way.
- It is the most important parameter of an SRAM cell

Data retention voltage
Data retention voltage could be explained as the lowest possible power supply voltage at which the data can be retained inside the SRAM. One thing to remember is that the chip is deselected at this point of time. It is typically in the order of 2V for a 5V part.

Read Delay
Read delay can be defined as the delay occurred while reading.

Write Delay
Write delay can be defined as the delay occurred while writing.

VI. APPLICATION

Static RAM exists primarily as:

General purpose products
- with asynchronous interface, such as the 28 pin 32Kx8 chips (usually named XXC256), and similar products up to 16 Mbit per chip
- with synchronous interface, usually used for caches and other applications requiring burst transfers, up to 18 Mbit (256Kx72) per chip

Integrated on chip
- as RAM or cache memory in microcontrollers (usually from around 32 bytes up to 128 kilobytes)
- as the primary caches in powerful microprocessors, such as the x86 family, and many others (from 8 kB, up to several megabytes)
- to store the registers and parts of the state-machines used in some microprocessors—see register file
- on application specific ICs, or ASICs (usually in the order of kilobytes)
- in FPGAs and CPLDs (usually in the order of a few kilobytes or less)

Embedded use
Many categories of industrial and scientific subsystems, automotive electronics, and similar, contain static RAM. Some amount (kilobytes or less) is also embedded in practically all modern appliances, toys, etc. that implement an electronic user interface. Several megabytes may be used in complex products such as digital cameras, cell phones, synthesizers, etc. SRAM in its dual-ported form is sometimes used for real-time digital signal processing circuits.

In computers
SRAM is also used in personal computers, workstations, routers and peripheral equipment: internal CPU caches and external burst mode SRAM caches, hard disk buffers, router buffers, etc. LCD screens and printers also normally employ static RAM to hold the image displayed (or to be printed). Small SRAM buffers are also found in CDROM and CDRW drives; usually 256 kB or more are used to buffer track data, which is transferred in blocks instead of as single values. The same applies to cable modems and similar equipment connected to computers.

Hobbyists
Hobbyists often prefer SRAM due to the ease of interfacing. It is much easier to work with than DRAM as there are no refresh cycles and the address and data buses are directly accessible rather than multiplexed. In addition to buses and power connections, SRAM usually require only three controls: Chip Enable (CE), Write Enable (WE) and Output Enable (OE). In synchronous SRAM, Clock (CLK) is also included.

VII. LITERATURE REVIEW

Analytic expressions for the SNM of R-load and full-CMOS SRAM cells have been derived. The expressions are useful in predicting the effect of parameters and operating conditions on the SNM as well as in optimizing the design of SRAM cells. In addition, an SNM simulation method which is quick and easy to use has been developed. The simulation results are in good agreement with the analytic SNM predictions. For the R-load cell, velocity saturation in real transistors causes some deviation. Further, it has been shown that full-CMOS cells have much better SNM values than R-load cells at low supply voltages. Therefore, in future memory processes, when the supply voltage has to be reduced to 3 V or less to avoid hot-carrier degradation, conventional R-load cells will suffer a significant disadvantage compared...
to full-CMOS cells. In order to maintain reasonable SNM values at a reduced supply voltage, the area required by R-load cells will be close to or equal to that of full-CMOS cells.[6]

New physical and stochastic models for 6T CMOS SRAM cell SNM are derived. These enable accurately assessing the impact of stochastic variations in device threshold voltage due to random placement of dopant atoms on cell stability by conjointly employing physical short-channel MOSFET drain current and threshold voltage roll-off models in tandem with stochastic models for intrinsic fluctuations of device threshold voltage. Stochastic distributions of cell SNM across the 1997 NTRS technology nodes calculated using these models demonstrate substantial reductions in cell SNM for sub-100-nm technology generations.[7]

Limit of SRAM data preservation under ultra-low standby VDD explored. An analytical model of the SRAM DRV is developed and verified with measurement results. A commercial SRAM module with high- Vth process is shown to be capable of sub-300mV standby data preservation. Under this low standby VDD, leakage power saving of more than 90% can be achieved with a dual-rail standby scheme designed for ultra low-power applications. The DRV is observed to be a strong function of process variation and SRAM cell sizing, while the design tradeoffs between read delay, area and leakage power can be optimized. While existing approaches generally involve significant tradeoffs with other performance metrics or technology limits, more opportunities exist on architectural level innovations. As an example, more SRAM leakage savings can be achieved with assistance from error tolerant schemes when the standby supply voltage is scaled down beyond the limit of DRV. Future work will be focused on exploiting design techniques to achieve even lower power and higher reliability in memory design.[8]

BM’s reliability program predicts SER values for various circuits in the appropriate use radiation environment. Accelerated testing illuminates the sensitivity to ionizing radiation sources that can cause soft errors. Monte Carlo simulations to predict the SER of devices given the actual product radiation environment used. Finally, life tests substantiate product SER estimates; since we conduct life tests at altitude and underground, predictions of both the alpha particle and cosmic ray SER components confirmed. From accelerated testing on bulk and SO1 SRAMs from the 90, 130 and 180 nm nodes [9].

A new 8T SRAM cell is presented, which reduces gate leakage in zero state significantly as compared to conventional 6T SRAM cell in caches. The proposed circuit is SNM free in read ‘0’ operation. There is, however, a 30% increase in cell area as compared to conventional 6T SRAM cell. Simulation results of 8T SRAM cell show a reduction of 46.2%, 50.2% and 9.8% in total leakage for the process TT, FF and SS respectively when cell stores logic ‘0’ in the standby mode. In this case, using high VT 8T SRAM cell, the total leakage is further reduced by 77%, 92% and 60% in process TT, FF and SS respectively. Simulation results for SNM show an improvement by 2.2 times when cell stores logic ‘1’ for read and standby mode operation [13].
VIII. CONCLUSION

SRAM is just one way to construct memory cells. SRAM uses six transistors per bit of storage, and is really fast. The six transistors per bit make large amounts of SRAM storage large and expensive though, so it is only applied in areas where the speed is critical, such as caches or local stores. Most processor caches are built from SRAM (the only exception that crosses my mind right now is the L3 cache in some Itanium monsters). It's entirely normal. SRAM is used in cache memory because it is so fast to access and can be accessed in a dual ported manner. The difference in the two applications is purely the manner of accessing data; in a cache, you access it by providing the/any address and get your data back whilst in the SPU you provide a raw address and do not hash it in anyway.

IX. REFERENCES