Imperial Journal of Interdisciplinary Research (IJIR)
Vol-2, Issue-7, 2016
ISSN: 2454-1362, http://www.onlinejournal.in

Design of BCH Decoder Based On Multi-bit Error Correction Codes Using VHDL

Mr. Anand N. Pachare[1], Prof. Sumit R. Vaidya[2] &
Mr. Sandip B. Pawar[3]
[1]M. Tech. Electronics (Communication) IV Sem. S.D.C.E. Selukate. Wardha.
[2]Assistant Professor, Department of Electronics and Communication Engineering
S.D.C.E. Selukate. Wardha
[3]Assistant General Manager, Uttam Value Steel Pvt. Ltd.,Selukate,Wardha

Abstract: *Error-correction codes are the codes used to correct the errors occurred during the transmission of the data in the undependable communication mediums. The idea behind these codes is to add redundancy bits to the data being transmitted so that even if errors occur due to noise in the channel, the data can be correctly received at the destination end point. Bose, Ray- Chaudhuri, Hocquenghem (BCH) codes are one of the error-correcting codes. Error detection is the detection of errors caused by the noise or other impairments during transmission from the transmitter to the receiver. It uses the concept of redundancy, which means adding of extra bits for detecting errors at the destination. In error correction the receiver can use any of the error-correcting code, which can automatically corrects certain errors and enables reconstruction of the original data. These can be done by means of digital filters by providing amount of delay for processing error detection and correction respectively. Over the duration, lots of techniques that make use of the filters structure and its properties to achieve fault tolerance have been proposed. Enhancing technology makes system more complex that include many filters. In those complex systems, it is frequent to have number of filters in circuit that functions in parallel architecture. In parallel combination of filters there apply the same filter to different input signals. So, from this case study the idea to implement parallel filters and digitally correct the errors are generalized. It has been proposed to protect digital signal processing circuits by using ECC i.e. Bose, Ray- Chaudhari, Hocquenghem (BCH) codes. The technique has evaluated using study on parallel infinite impulse response filters making effectiveness in terms of protection and implementation cost. The enhanced BCH decoder is designed using hardware description language called Verilog and synthesized in Xilinx ISE Tools 13.2.*

Keywords*- FIR (Finite Impulse Response) filter, IIR (Infinite Impulse Response) filter*

1. Introduction

The filters are mainly used to reject unwanted components in order to provide better quality signal at the output. These filters are playing vital role in the signal processing and communication system image enhancement noise and echo cancellation etc. there are two main types of filters, they are analog and digital. In Analog filter the output and input are the analog signal. Even though these filters are fast and simple to realize, they are little in stable. So now a day the analog filters are replaced with the digital filters because of performing the numerical calculation on sampled signal value and also these filters are further classified into two types:

- FIR (Finite Impulse Response) filter
- IIR (Infinite Impulse Response) filter

The FIR filter is preferred over the IIR filter because of efficient implementation with fewer finite precision errors and having better stability with linear phase. The objective used, enhancing the individual block the speed in the digital system lead to the enhancement of the overall system speed. The three different pipelined structures-1; fine grain and broadcast are used for designing the IIR filter. These can be synthesized using the Xilinx synthesis tool and can be implemented using the Spartan 3A FPGA family. These experiments generate the result that the fire grain structure is used for the effective area utilization, and the pipelined structure-1 structure used for the speed operation.

The digital filters are more flexible and as the ability to process the signal in various ways and it also as the ability to adapt the changes in the characteristics of the signal. Pipelining is the technique called overlapping of various instructions during execution. By using this technique the optimized speed and the minimal hardware fair of the FIR filter design is being achieved. Also by using this technique the delay at the filter is to be reduced on comparing with the non pipelined structure [7]. The tapped line delay structure and the transposed

filter structure have been studied and the filter is also implemented with the Separated arithmetic and symmetric convolution technique. The better solution for the realization of the filters is the multistage digital filter. By combining the decimation /interpolation operations related to the implementation of multi channel filter in the pipelining interleaving technique can give an efficient multistage multichannel digital filter. In the brief, this paper gives the implementation of efficient pipelined filter also further achieving a fault tolerant reliable operation by implementing this filter with the redundant module.

A fault in a system is some deviation from the expected behavior of the system: a malfunction .Faults may be due to a variety of factors, including hardware failure, software bugs, operator (user) error, and network problems. If we look at the words fault and tolerant, can define the fault as a malfunction or deviation from expected behavior and tolerant as the capacity for stable or putting up with something. Putting the words together, fault tolerance refers to a system's ability to deal with malfunctions. Fault tolerant is the realization that we will always have faults (or the potential for faults) in our system and that we have to design the system in such a way that it will be tolerant of those faults.

II. Related Work

In this paper we have used the FIR filter for error detection and correction. In that paper the main block diagram which consisting of BCH decoder and FIR filter. The BCH decoder consisting of syndrome, chein search and error correction. The FIR filter which consisting of multiple constant multiplication, adders and flip flops. In first module we have generating only the BCH decoder the data bits which are to be provided to syndrome block which is to be stored in the registers or the memory.

III. Proposed Methodology

The proposed work consisting of the different data or the signals which is to be providing. By the use of FIR filter we can detect the errors and corrected up to high levels. The figure below which shows that the overall working of the module.

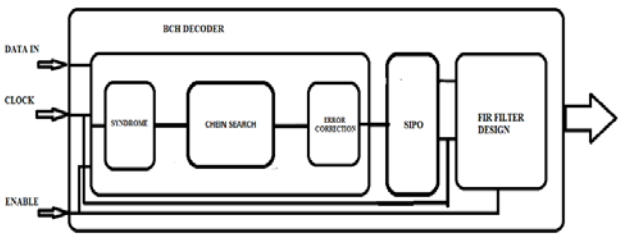

Fig 1. Block Diagram

The BCH decoder shown in figure below has three blocks namely: syndrome calculator, Chien search and error correction. The Bose, Chaudhuri, and Hocquenghem (BCH) codes form a large class of powerful random error-correcting cyclic codes.

Syndrome Calculator:

The syndrome calculator is the first module at the decoder, the design of this module is almost same for all the BCH decoder architectures. The important characteristics of the syndrome are that they depend on only error location not on the transmitted information.

Chien Search:

The IBM block outputs are the inputs to the chien search block which generates 15 bit results that shows the exact position where the errors are present. a,b,c,d in the above figure 8 are the chien search block inputs each of 4 bits and y[14:0] is the 15 bit output which shows the exact error location.

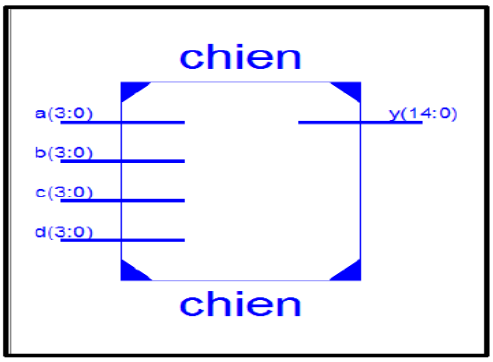

Fig 2. Chien Search

Error Correction:

Here the chien search output is EX-ORed with the received data that gives the output which is the uncorrupted data.

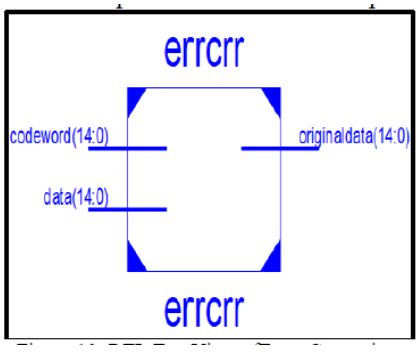

Fig. 3 Error Correction

The received corrupted input at the decoder and codeword which is the output of the chien search are the inputs to the error-correction block which gives uncorrupted original data as the output.

IV. Simulation Results

Simulation is carried out using Xilinx ISE 13.2 design suit tool.

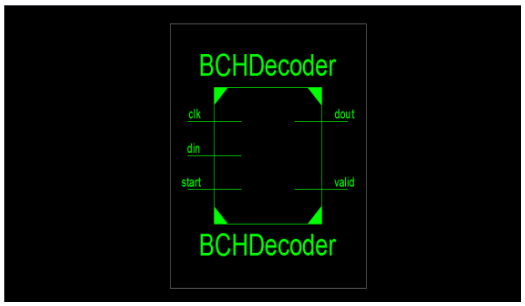

Fig. 4 RTL Top view of BCH Decoder

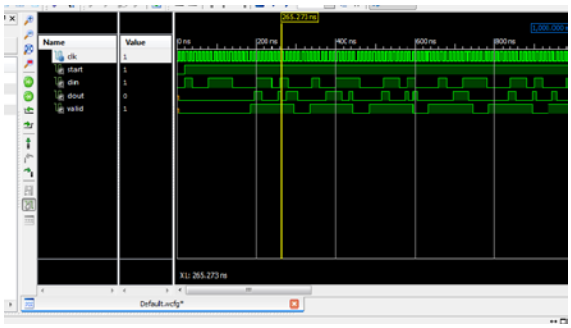

Fig. 5 Output Simulation Test-bench Waveform

V. Conclusion

Proposed work is likely to achieve FIR filters using multi-bit error correcting codes and also to obtain low complexity, reduce delay and area efficient protection technique for higher bits data using VHDL.

VI. Future Scope

In future work we have to design FIR filter. The FIR filter which is consisting the different blocks like as multiple constant multiplications, adders and the flip flops by the use of these blocks we have to obtaining the corrected and the error free data.

Reference

[1]"Fault Tolerant Parallel Filters Based on Error Correction Codes", Zhen Gao, Pedro Reviriego, Wen Pan, Zhan Xu, Ming Zhao,Jing Wang, and Juan Antonio Maestro, IEEE Transactions On Very Large Scale Integration (Vlsi) Systems.

[2] "Area Efficient and Fault Tolerant FIR Filter", Brajesh Kumar Gupta (nit Jamshedpur), Associate prof. R. Sinha (nit Jamshedpur)

[3] "Fault-Tolerant Computation within Complex FIR Filters." P. Chan, G.A. Jullien, L. Imbert, V.S. Dimitrov, G.H. McGibney.

[4] "Optimization of Self Checking FIR filters by means of Fault Injection Analysis", S. Pontarelli, L. Sterpone, G.C. Cardarilli, M. Re, M. Sonza Reorda, A. Salsano, M. Violante.

[5]B. Shim and N. Shanbhag, "Energy-efficient soft error-tolerant digital signal processing," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 14, no. 4, pp. 336–348, Apr. 2006.

[6]R. W. Hamming, "Error correcting and error detecting codes," Bell Syst. Tech. J., vol. 29, pp. 147–160, Apr. 1950.

[7]T. Hitana and A. K. Deb, "Bridging concurrent and non-concurrent error detection in FIR filters," in *Proc. Norchip Conf.*, 2004, pp. 75–78.

[8] Y.-H. Huang, "High-efficiency soft-error-tolerant digital signal processing using fine-grain sub word-detection processing," IEEE Trans. Very Large Scale Integer. (VLSI) Syst., vol. 18, no. 2, pp. 291–304, Feb. 2010.

[9]S. Pontarelli, G. C. Cardarilli, M. Re, and A. Salsano, "Totally fault tolerant RNS based FIR filters," in *Proc. IEEE IOLTS*, Jul. 2008, pp. 192–194.

[10]Z. Gao, W. Yang, X. Chen, M. Zhao, and J. Wang, "Fault missing rate analysis of the arithmetic residue codes based fault-tolerant FIR filter design," in Proc. IEEE IOLTS, Jun. 2012, pp. 130–133.