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Design and Implementation of CMOS Based Digital Circuit

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Abstract*: Make use of a simple CMOS IC fabrication procedure that has been not long ago execute at the Microelectronics Research Centre (MRC), this project will focus on designing and implementation a CMOS circuit. The primary target is to focus test the practicality of using the CMOS process for building practical IC's at the MRC. Dedicated the design group will design, fabricate, and test a IC. Suppose product will be a report relates how the actual circuit accomplish in comparison to design simulations. This is significant to the MRC for future learner to earning experience designing and implementing contemporary IC'*

Introduction

Complementary metal oxide semiconductor (CMOS) circuitry (chip) is the authorizing electronic component for the current information age. Because of their inherent characteristics in low-power consumption, large noise margins, simple to design , CMOS integrated circuits have been universally used to establish random access memory(RAM) chips, and applications-specific integrated circuit (ASIC) chips . The popular way of CMOS circuits will evolve with the growing applications for low power, low-noise integrated electronic systems in the progress of portable computers, personal digital assistants (PDAs), portable phones, and multimedia agents.

The auto-electronic management has attained a phenomenal growth accomplished the final few decades, mainly as the fast advances in integration technologies and large-scale systems design. The benefit of IC chip in high-performance computing, telecommunications, and consumer electronics has been growing day by day. Frequently, the necessary computational and information processing power of the mentioned functions is the driving force for the fast development of this field. The current leading edge technologies (like low bit-rate video and cellular communications) already arrange the end–users a certain amount of processing power and flexibility. This trend is expected to continue, with very important implications for VLSI and systems design. One of the better characteristics of information services is their increasing need for very high processing power and bandwidth (in order to handle real-time video, for example). The other most important characteristic is that the information services tend to become more personalized, which means that the information processing devices must be more intelligent and be portable to allow more mobility. This trend towards portable, distributed system architectures is one of the main driving forces for system integration, although it does not inhibit a concurrent and equally important trend towards centralized, highly powerful information systems such as those required for network computing (NC) and video services. As more and more complicated functions are necessary in different data processing and telecommunications devices, the need to integrate these functions in a small package is also increasing. The level of integration as steady by the number of logic gates in a monolithic chip has been immovably increasing for almost three decades, mainly due to the fast gain in processing technology and interconnects technology.

1.1) Basic Logic Gates

The most basic elements of digital circuits are the logic gates. The most basic types of electronic circuit designed with active devices(such as diodes, transistors) and passive components (such as resistors) which consist of two or more inputs and one output performing very basic logic operation are known as the logic gates.

There are seven types logic gates namely OR, AND, NOT, NOR, NAND, EX-OR, and EX-NOR. First three gates are known as basic types of gates while NAND and NOR gates are called universal gates.

1) OR gate

The OR gate performs logical addition, more commonly known as the OR function. An OR gate has two or more input signals with only one output signals. The Boolean equations for logical OR gate is given by this expression

Z= A +B

2) AND Gate The AND gate performs logical multiplication, more commonly known as AND function. The AND gate has two or more inputs and a single output, as shown by the standard logic symbols. The AND gate provides high output only when all inputs are high. The Boolean equation for logical AND is given by this expression

$$Z = A \cdot B$$

NOT GATE

The inverter (NOT circuit) performs a basic logic function called inversion or complementation. The purpose of the inverter is to change one logic level to the opposite level. In terms of bits, it changes a 1 to a 0 and vice versa. This gate has only one input and one output. NOT gate is called inverter because output state is always opposite to the input state, so when the input is low signal, output signal is high and vice-versa.

The Boolean expression for OR gate is given by this expression

$$Z = \overline{A}$$

NAND gate

The term NAND is a contraction of NOT-AND and implies an AND function with complemented (inverted) output. In this output is low only when all inputs are high. NAND gate operates like an AND gate followed by an INVERTER.

The Boolean expression for NAND gate is given by this expression

$$Z = \overline{A \cdot B}$$

Circuit Design Using Cadence EDA Tool

STARTING THE CADENCE SOFTWARE

Use the UMC_180nm design kit for this training

1) Change to the directory, where the UMC_180nm design kit is installed. Check whether the cds.lib file is placed in your present working and contains all the required library paths.cds.lib file is the local initialization file. The library search paths are defined in this file.

2) In the same terminal window, enter:

> icfb &

The icfb or Command Interpreter Window (CIW) appears at the bottom of the screen.

.1) **SCHEMATIC ENTRY**

OBJECTIVE:-To create a new cell view and build desired circuit. Below steps explain in creation of new library "training" and we will use the same throughout this course for building various cells.

CREATING A NEW LIBRARY

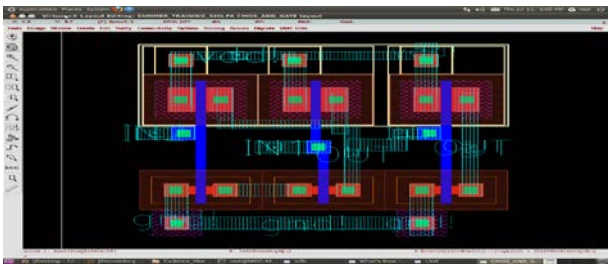
1) In the Library Manager, execute File-New-Library. The new library form appears.

2) In the "New Library" form, type Training in the Name section.

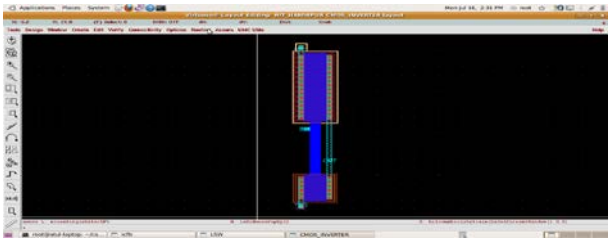
3) In the field under the Directory section, verify that the path to the library is set to the present working directory and click OK.

4) In the "Technology File for New library" form, select option Attach to an existing techfile and click OK

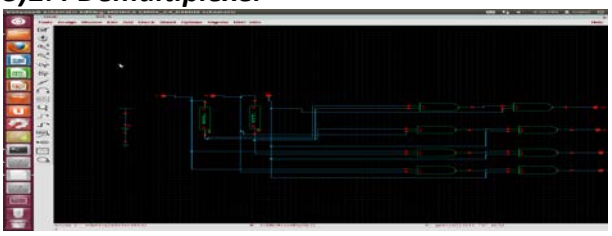
1) AND GATE

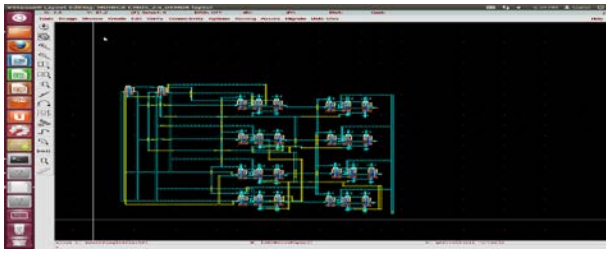


2.NOT GATE

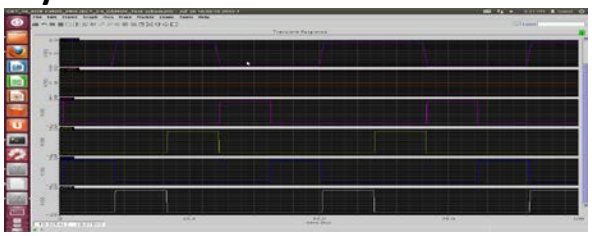


3)2:4 Demultiplexer





Layout



Result

Circuits using CMOS technology are designed. CMOS based 2:4 demultiplexer circuit has been designed using Cadence EDA Tool. With the help of this technology I have designed 2:4 demultiplexer circuit using AND,NOT. As we know CMOS a complementary metal oxide semiconductor device is basically a combination of PMOS AND NMOS so we have used these devices in making our circuit. . I have also generated "gds" file for our project. For fabricate of our circuit into IC's, gds file is only needed.

Conclusion

The primary goal of this thesis work is not only to provide an efficient result in low power VLSI design but also shows a successful try in terms of reduction of power dissipation. The basic low power CMOS cell structures as like a two- input AND gate, a two-input OR gate, a two-input XOR gate etc are designed using complementary CMOS logic style technique. The entire CMOS cell structures which are designed in this thesis work are designed in Cadence IC Design Architect using standard TSMC 0.18µm technology. Because of the main concern is power dissipation so after the schematic design and the simulation, different value of power dissipation at different frequencies has been taken for both the logic style and compared with each other. All the circuits operate at a supply voltage of 1.8 V and load capacitance is varied according to the circuit design.

Future Scope of Work

1) This technique can be used to design low power circuits such as digital wrist watches, radio frequency identification, sensor nodes, laptops, and battery operated devices such as cellular phones etc.

2) This thesis work is based on combinational circuit design so there is a highly fill place for the sequential circuit design for providing a better design. In low power VLSI design this technique has a very good scope for future.

References

1. Sung-Mo kang, Yusuf lablebici, “CMOS DIGITAL INTEGRATED CIRCUITS: Analysis and Design”, 3rd edition Tata Mc-Graw Hill, 2003
2. John P. Uyemura “Introduction to VLSI Circuits and Systems”, Wiley, John & Sons, Inc., 2002.
3. R. J. Baker, H. W. Li, and D. E. Boyce, “CMOS circuit design, layout, and simulation,” IEEE Press series on Microelectronic Systems.
4. N. Weste and K. Eshraghian, “Principal of CMOS digital design”, 2nd edition, Pearson Education, 2005.
5. Douglas A. Pucknell and Kamran Eshraghian, “Basic VLSI Design” 3rd edition Prentice Hall of India, 2005.