Imperial Journal of Interdisciplinary Research (IJIR)
Vol-2, Issue-5, 2016
ISSN: 2454-1362, http://www.onlinejournal.in

Comparative Study of Performance of Different Multipliers

Deepika Sharma[1], Ruchi Garg[2], Yogita Wadhwa[3]
[1,2,3](ECE Department, M.M. University Sadopur, Ambala)

Abstract: *To accomplish the better execution in most of the real time and information handling, arithmetic operations having higher throughput are fundamental. Multiplication is a principle arithmetic operation required in these approaches and the advancement in higher speed multiplier circuit has been an area of interest over a long period. Time delay and power consumption reduction are necessary in many applications. It is constantly important to plan a quick multiplier in VLSI in order to upgrade system performance. In this paper, we have examined distinctive sorts of multipliers such as Array multiplier, Wallace tree multiplier, Modified Booth multiplier, Modified Booth-Wallace tree multiplier in light of different parameters like speed, area and power consumed. Every multiplier has its own particular points of interest and inconveniences.*

Keywords
Array Multiplier, Wallace tree Multiplier, Modified Booth Multiplier, Modified Booth-Wallace tree Multiplier

I. INTRODUCTION

Now a day's multipliers perform an important role in digital signal handling and different types of applications. In elite frameworks, for example, microprocessor, DSP and so forth addition and multiplication of binary numbers are principal and regularly utilized in arithmetic operations. Most of the instructions in microprocessor and a large portion of DSP calculations execute operation of addition and multiplication [1]. In this way, these operations dominate the implementation time [2]. That is the reason, there is a necessity of fast multiplier.

In computer and data processing applications requirement of fast processing has been increased [3], [4]. Low power utilization is additionally a critical matter in multiplier configuration with need of fast multiplier. High speed and low power utilization unit is the goal of an efficient multiplier [6]-[8].

Multipliers can be grouped into serial and parallel multipliers [9]. In serial multiplier, every bit of multiplier is utilized for assessing the partial products while in parallel multipliers, partial product from every bit of multiplier is figured in parallel [10], [11]. Contingent upon the sort of utilization parallel or serial multiplier can be utilized[12].

II. ARRAY MULTIPLIERS

Array multiplier is familiar because of its normal construction. Circuit of Multiplier depends upon repeated addition and shift system [15]. This multiplier performs multiplication by the standard add and shift operation utilizing add and shift algorithm [16]-[18]. Partial products are created by multiplying the multiplicand with every bit of the multiplier. The partial products acquired are then shifted relying upon their bit arrangement and are at long last added at the last stage [14]. The number of partial products that are created is equivalents to number of multiplier bits. Array Multiplier has more power consumption and additionally ideal number of components needed, yet delay in this multiplier is bigger [13]. Large number of gates requirement leads to increase in area [2] [10]. So, this is a high speed multiplier having complex hardware.

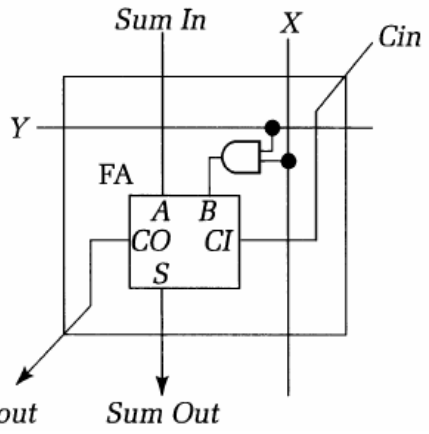

Fig.1 Basic building blocks of an Array Multiplier.

III. WALLACE TREE MULTIPLIER

A proficient hardware execution of a digital circuit to multiply two integer numbers is Wallace tree Multiplier [19]. In 1964, it is contrived by an Australian computer scientist Chris Wallace. Number of partial products will get decrease by this multiplier. It has four data input lines D0, D1, D2, D3 that should be added and has two outputs Carry and Sum which are supposed consequence of compressor [20]. As shown in Fig2, The two extra lines represent the previous and generated carries. A 4:2 compressor consists of two full adders(FA) connected in arrangement as appeared in Figure 2

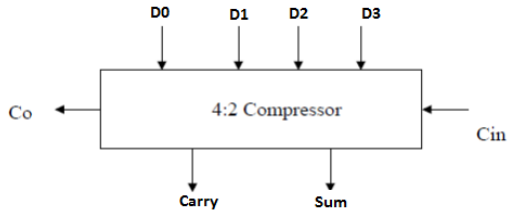

Fig. 2: Block diagram of 4:2 Compressor [21]

A reduction approach for the addition of partial products is Wallace tree multiplier that uses the carry save adder. Figure 3 shows a block diagram that consists of a tree architecture for the data distribution that utilize 4:2 compressors.

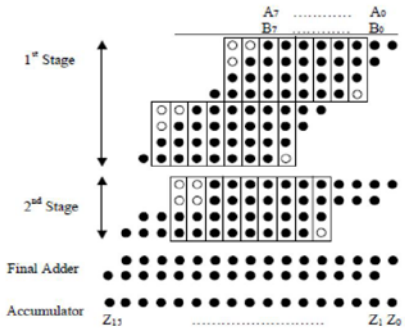

Figure 3: A tree architecture in Wallace Multiplier for data distribution [20].

Every box has bits that are required to insert in 4:2 compressor [21]. Quantity of partial items can be deceased by the two phases of 4:2 compressors in proportion of 2:1. The tree architecture shown in figure exhibits the two operands that is formed by the reduction of 8 partial products, that are then summed together and forming final product with the help of fast carry propagate adder. 4:2 compressor has basic and well ordered connection of multiplier tree.

IV. MODIFIED BOOTH MULTIPLIER

The Modified Booth multiplier is that multiplier which scans the three bits at once to decrease quantity of partial products [13]. The Modified Booth multiplier configuration utilizes a modified Booth encoder and selector procedure to reduce and reorder partial products. This decreases the number of gates count and enhances the multiplier's performance. Modified Radix-4 Booth algorithm is generally used when operands are equal or greater than 16 bits [22].

Bits of Multiplier	**Digit of Signed Multiplier**
000	0
001	+1* Multiplier
010	+1* Multiplier
011	+2* Multiplier
100	-2* Multiplier
101	-1* Multiplier
110	-1* Multiplier
111	0

Table 1: Radix-4 Booth's recording for all possible blocks [17]

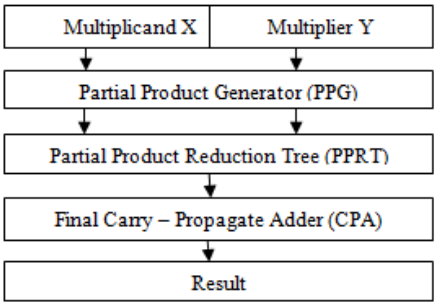

Fig 4: Flowchart of Modified Booth Multiplier

For high speed multiplication Booth algorithm performs many steps of multiplication. In the multiplicand and multiplier if the consecutive bits are same then it has been proved by the booth multiplication that addition and subtraction can be omitted. In this way in the greater part of the cases delay of Booth Multiplication is littler than that of Array Multiplier. However Booth Multiplier's performance for delay is reliant on input data.

The elite of booth multiplier accompany the disadvantage of power consumption due to usage of expansive number of adder cells required that expends extensive power [13].

V. MODIFIED BOOTH-WALLACE TREE MULTIPLIER

Modified Booth-Wallace tree multiplier comprises of four main modules that are Wallace tree, Booth encoder, carry look-ahead adder and partial product generator [7]. Partial products are produced that depend on the multiplicand and encoded multiplier. For multiplier of 64 bits, the performance of Modified Booth algorithm is restricted. So Booth multiplier with Wallace tree structures has been utilized to make it fast multiplier [8]. Partial products are then further given to Wallace Tree and then summed properly. A fast adder, that is, Carry Look-ahead Adder (CLA) is used for getting the final result as shown in fig 5:

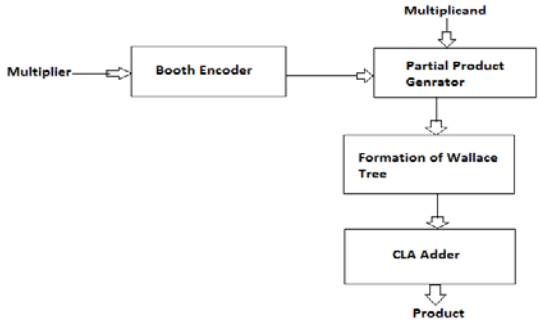

Fig 5: Block Diagram of Modified Booth Wallace tree multiplier.

Modified Booth Algorithm is utilized to save chip area instead of reducing delay time and Wallace tree operation time is used to decrease the delay because it makes utilization of Carry Save Adders (CSA) for fast accumulation of the partial products. By utilizing Wallace tree multiplier, power consumption too is reduced when contrasted and different multipliers. For further increasing speed, carry look-ahead adder is utilized as final adder.

VI. CONCLUSION

Four multipliers studied above are analyzed by considering speed, area and power. The fundamental Array multiplier is the most straightforward of all multipliers in its circuit complexity and subsequently involves a very small area but these multipliers perform multiplication at a low speed utilizing the fundamental add and shift operation and have large power consumption.

It can be reasoned that of the considerable number of multipliers, Modified Booth Wallace tree multiplier is the quickest as it exploits both multipliers, that is, Modified Booth multiplier wherein the number of partial products are decreased by 50% or 33% of the multiplier bits taking into account the calculations it uses.

Parameters	Array Multiplier	Wallace tree Multiplier	Modified Booth Multiplier	Modified Booth-Wallace tree Multiplier
Speed	Low	Higher	High	Highest
Area	Small	Large	Medium	Largest
Power	Highest	High	Less	High

REFERENCES

1. Kantabutra, “Designing Optimum One-Level Carry-Skip Adders”, IEEE Transactions on Computers, pp.759-764, June 1993.
2. Koc, C.K., “RSA Hardware Implementation”, RSA Laboratories, RSA Data Security, Inc. 1996.
3. Goel. A., and Bapat, P., "A New Time-Position Algorithm for the Modeling of multilevel Carry Skip Adders in VHDL", Canadian Conference on Electrical and Computer Engineering, pp. 158-61, 1996.
4. Oklobdzija, V.G.; Villeger, D.; Liu, S.S.; “A method for speed optimized partial product reduction and generation of fast parallel multipliers using an algorithmic

approach" IEEE Transactions on Computers, vol.45, pp 294 – 306, 1996.
5. R. Zimmermann, "Binary Adder Architectures for Cell-Based VLSI Synthesis", A dissertation submitted to the Swiss Federal Institute of Technology, Zurich for the degree of Doctor of technical sciences, 1997.
6. Neil. H. E. Weste , "Principle of CMOS VLSI Design", Adison-Wesley, 1998.
7. K.C. Chang, "Digital system design with VHDL and Synthesis" An integrated Approach IEE Computer Society, pp 408-437, 1999.
8. B. Parhami, "Computer Arithmetic, Algorithm and Hardware Design", Oxford University Press, New York, pp.73-137, 2000.
9. Weng Fook Lee, "VHDL Coding and Logic Synthesis with Synopsys" Academic Press pp.147-227, 2000.
10. A. A. A., Gutub and H. A., Tahhan, "Efficent Adders to Speedup Modular Multiplication for Cryptography", Computer Engineering Department, KFUPM, Dhahran, SAUDI ARABIA, 2001.
11. Fayed, Ayman A., Bayoumi, Magdy A., "A Merged Multiplier-Accumulator for high speed signal processing applications", IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP), pp 3212 - 3215, 2002.
12. Deschamps, J.P.; Bioul, G.J.A; Sutter,G.D.; "Synthesis of Arithmetic Circuits"; ASIC and Embedded Systems, John Wily & Sons Inc., Publication, 2006.
13. Jung-Yup Kang, Member, IEEE, and Jean-Luc Gaudiot, Fellow, IEEE Transaction on Computers, Vol. 55, No. 10, October 2006.
14. Abdelgawad, A., Bayoumi, M., "High Speed and Area-Efficient Multiply Accumulate (MAC) Unit for Digital Signal Processing Applications", IEEE International Symposium on Circuits and Systems, pp. 3199 – 3202, 2007.
15. Naofumi Homma, Member, IEEE, Takafumi Aoki, Member, IEEE, and Tatsuo Higuchi, Life Fellow, IEEE Transaction on Computers, Vol. 57, No. 12, December 2008.
16. R.P.P., Singh; B. Singh and P. Kumar, "Performance Analysis Of Fast Adders Using VHDL", International Conference on Advances in Recent Technologies in Communication and Computing, 2009.
17. Kim Soojin; Cho Kyeongsoon; "Design of High-speed Modified Booth Multipliers Operating at GHz Ranges", World Academy of Science, Engineering and Technology, Issue 61, January 2010.
18. P. Devi and A. Girdher, "Improved Carry Select Adder with Reduced Area and Low Power Consumption", International Journal of Computer Applications (0975–8887) vol. 3 – No.4, June 2010.
19. Jiun-Ping Wang, Shiann-Rong Kuang, Member, IEEE, and Shish-Chang Liang, IEEE Transaction on Very Large Scale Integration (VLSI) Systems, Vol. 19, No. 1, January 2011.
20. S.Jagadeesh, S.Venkata Chary, International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622, Vol. 2, issue 5, pp.425-431, September-October 2012.
21. H. S. Krishnaprasad Puttam, P. Sivadurga Rao & N. V. G. Prasad3, International Journal of Modern Engineering Research (IJMER), Vol. 2, Issue. 5pp-3390-3397 ISSN: 2249-6645, Sep.-Oct. 2012.
22. International Journal of VLSI and Embedded Systems-IJVES, ISSN: 2249 – 6556 Vol. 04, Issue 02; March - April 2013.