A Hybrid Filter for the Suppression of Common-Mode Voltage and Differential Mode Harmonics in Three-Phase Inverters with CPPM

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Abstract—In the motor systems driven by sinusoidal pulse width modulation (SPWM) three-phase inverters, the peaks of common-mode (CM) voltage are so high that it will cause many negative effects. In this paper, a hybrid filter is presented to reduce the CM voltage (CMV) and the differential-mode (DM) harmonics in a three-phase inverter with carrier peak position modulation (CPPM). Because the use of CPPM strategy in the inverter can ensure that the output CMV will be only two levels in any condition, the simple active CM filter (composed of a half-bridge circuit) in the hybrid filter can effectively suppress the output CMV and CM current. The passive filter in the hybrid filter consists of an added single tuned filter and the original DM low-pass filter. The single tuned filter is designed to lower the DM harmonics, which are aggravated by the CPPM strategy in the carrier frequency band. Through the experiments, the validity of CMV and DM harmonics suppression by the hybrid filter in the three-phase inverter is verified and the calculation-control active CM filter is proved to be the best in the optional schemes.

Index Terms—Carrier peak position modulation (CPPM), common-mode voltage (CMV), differential-mode (DM) harmonics, hybrid filter, sinusoidal pulse width modulation (SPWM).

I. INTRODUCTION

SWITCHED-MODE power supplies are more and more widely used in industrial equipments. But this switched mode will bring many negative effects. In the motor regulation Systems driven by pulse width modulation (PWM) inverters, the peaks of output common-mode (CM) voltage are very high due to the instantaneous imbalance of three phase voltages. The CM voltage (CMV) will produce a huge pulsating CM current (CMC) through the distributed capacitance of the system. The CMC could interfere with the adjacent devices along the ground wire and even will result in the wrong operation of the devices [1], [2]. In addition, the CMV will cause the high shaft voltage through the parasitic capacitors between the stator and the rotor. The high shaft voltage could lead to momentary electromagnetic discharge phenomena (viz. the bearing current) [3]–[5] and will therefore damage the motor bearing [6], [7].

In recent studies, some optimized control strategies are used to reduce the output CMV in the three-phase inverter. For the inverter with the space vector modulation (SVM) strategy, the CMV is reduced by using nonzero vectors to synthesize zero vectors [8]–[10]. For the inverter with the discontinuous PWM (DPWM) strategy, the CMV is reduced by avoiding the generation of zero vectors. In this method, three triangular carriers with various polarities are used to modulate three reference voltages. Under different carrier polarity combinations there are different DPWM methods [11], [12], such as active zero state PWM (AZSPWM) [13], remote state PWM (RSPWM) [14], [15], near state PWM (NSPWM) [16], and so on. For the sinusoidal PWM (SPWM) control inverter, the CMV can be reduced by using the carrier phase shift (CPS) strategy [17]. But in the application of the CPS strategy, the modulation index $Ma$ of SPWM must be limited to $Ma < 2/3$. In order to break through the limitation of the modulation index, the strategy of carrier peak position modulation (CPPM) is adopted [18]. When the zero state appears, instead of the usual symmetric triangular carrier, an oblique triangular carrier is used to modulate the reference voltage. Thus, the zero state is avoided and the CMV is reduced.

In the inverter system, the peak value of the output CMC is influenced by the CMV $dv/dt$ and the distributed capacitance of the system. When the system is established, the CMV $dv/dt$ plays a decisive role in the CMC. In aforementioned strategies, although all the output CMVs of inverters can be reduced to $V_{dc}/6$ ($V_{dc}$ is the dc-side voltage of inverters), the step level of CMV is still $V_{dc}/3$ when their switches are switching. So the peak of CMC will not be reduced. Only with the aid of a CM filter could more CMV and CMC be reduced. CM filters can
be divided into passive and active ones. Most passive filters are realized with two common ways: a CM choke [19]-[21] or CM transformer [22]-[24] cascading into the main circuit; a resistor-capacitor (RC) or resistor-inductor-capacitor (RLC) attenuation network paralleling into the main circuit [25]-[27]. The drawbacks of passive CM filters are as follows: its bulky size, high power loss, etc.

Active CM filters are of more popular concern. In some active filters, the active devices are working in the linear region and the reversal voltage is produced to compensate the CMV of the three-phase inverter [28]-[30]. Although the suppression effect of CMV is excellent under this method, it is difficult to implement this type of filters in high-voltage cases because of the linear area restriction for analog push-pull transistors.

The active power filter composed of switching circuits is not affected by the limit of voltage class. In the conventional SPWM or SVM three-phase inverter, the CMV is a four-level pulse. So the active filter is implemented by using a multi-level inverter and the four-level voltage is yielded to counteract the CMV [31]. The structure of this multi-level active filter is too complex to be used in the low cost cases. In the above active filters, all the compensative voltages are cascaded into the inverter’s output through a CM transformer. The CM transformer is complex in design and manufacture, big in size, and not easy to be installed because of the cascade mode, which is especially not propitious for the revamping of the established inverter. In the inverter with CPS, the CMV is suppressed by using three-phase four-leg topology [17]. Because the modulation index under the CPS strategy is limited, the application of this filter is restricted.

1.1 HARMONICS

The typical definition for a harmonic is “a sinusoidal component of a periodic wave or quantity having a frequency that is an integral multiple of the fundamental frequency.”. Some references refer to “clean” or “pure” power as those without any harmonics. But such clean waveforms typically only exist in a laboratory. Harmonics have been around for a long time and will continue to do so. In fact, musicians have been aware of such since the invention of the first string or woodwind instrument In order to be able to analyze complex signals that have many different frequencies present, a number of mathematical methods were developed. One of the more popular is called the Fourier Transform. However, duplicating the mathematical steps required in a microprocessor or computer-based instrument is quite difficult. So more compatible processes, called the FFT for Fast Fourier transform, or DFT for Discrete Fourier Transform, are used. These methods only work properly if the signal is composed of only the fundamental and harmonic frequencies in a certain frequency range (called the Nyquist frequency, which is one-half of the sampling frequency).

1.2 EFFECTS OF HARMONICS

The presence of harmonics does not mean that the factory or office cannot run properly. Like other power quality phenomena, it depends on the “stiffness” of the power distribution system and the susceptibility of the equipment. Equipment that can have mis-operations or failures due to high harmonic voltage and/or current levels. In addition, one factory may be the source of high harmonics but able to run properly. This harmonic pollution is often carried back onto the electric utility distribution system, and may affect facilities on the same system which are more susceptible. Some typical types of equipment susceptible to harmonic pollution include, Excessive neutral current, resulting in overheated neutrals. The odd triplen harmonics in three phase wye circuits are actually additive in the neutral. This is because the harmonic number multiplied by the 120 degree phase shift between phases is an integer multiple of 360 degrees. This puts the harmonics from each of the three phase legs “in-phase” with each other in the neutral, as shown in Figure.
Incorrect reading meters, including induction disc W-hr meters and averaging type current meters.

Reduced true PF, where PF = Watts/VA.

Overheated transformers, especially delta windings where triplen harmonics generated on the load side of a delta-wye transformer will circulate in the primary side. Some type of losses go up as the square of harmonic value (such as skin effect and eddy current losses). This is also true for solenoid coils and lighting ballasts.

Zero, negative sequence voltages on motors and generators. In a balanced system, voltage harmonics can either be positive (fundamental, 4th, 7th,...), negative (2nd, 5th, 8th...) or zero (3rd, 6th, 9th,...) sequencing values. This means that the voltage at that particular frequency tries to rotate the motor forward, backward, or neither (just heats up the motor), respectively. There is also heating from increased losses as in a transformer. Nuisance operation of protective devices, including false tripping of relays and failure of a UPS to transfer properly, especially if controls incorporate zero-crossing sensing circuits.

Bearing failure from shaft currents through uninsulated bearings of electric motors.

Blown-fuses on PF correction caps, due to high voltage and currents from resonance with line impedance.

Mis-operation or failure of electronic equipment.

1.3 SOURCES OF HARMONICS:

How this electricity is used by the different type of loads can have an effect on “purity” of the voltage waveform. Some loads cause the voltage and current waveforms to lose this pure sine wave appearance and become distorted. This distortion may consist of predominately harmonics, depending on the type of load and system impedances.

“The main sources of harmonic current are at present the phase angle controlled rectifiers and inverters.” These are often called static power converters. These devices take AC power and convert it to another form, sometimes back to AC power at the same or different frequency, based on the firing scheme. The firing scheme refers to the controlling mechanism that determines how and when current is conducted. One major variation is the phase angle at which conduction begins and ends.

1.4 SOLUTION FOR HARMONICS

Care should be undertaken to make sure that the corrective action taken to minimize the harmonic problems don’t actually make the system worse. This can be the result of resonance between harmonic filters, PF correcting capacitors and the system impedance. Isolating harmonic pollution devices on separate circuits with or without the use of harmonic filters are typical ways of mitigating the effects of such. Loads can be relocated to try to balance the system better. Neutral conductors should be properly sized according to the latest NEC-1996 requirements covering such. Whereas the neutral may have been undersized in the past, it may now be necessary to run a second neutral wire that is the same size as the phase conductors. This is particularly important with some modular office partition-type walls, which can exhibit high impedance values. The operating limits of transformers and motors should be derated, in accordance with industry standards.
from IEEE, ANSI and NEMA on such. Use of higher pulse converters, such as 24-pulse rectifiers, can eliminate lower harmonic values, but at the expense of creating higher harmonic values.

II. PROPOSED TOPOLOGY

HYBRID FILTER

In this paper, the primary task of the designed filter is to suppress the output CMV in the three-phase inverter. Using the CPPM strategy can ensure that the output CMV will be only two-level voltage in any case (see Section II). Thus, to suppress the CMV, a simple switching circuit can be designed as an active CM filter to produce the two-level voltage, which is the reversal of the original CMV. Meanwhile, a special design of DM filter aims at the suppression of the DMV harmonics in the carrier frequency band, because the DMV harmonics will make the THD exceed the standards (see Section III). The organic combination of the active CM filters and the passive DMV filter forms the hybrid filter in this paper.

A. Active CM Filter

In the design procedure of the active CM filter, the switching circuit structure must be determined in accordance with the characteristic of the CPPM strategy firstly. Secondly, the coupling mode of the filter output must be designed. Lastly, the acquisition mode of the CMV signal must be selected.

Because the output CMV in the inverter with CPPM is a twolevel voltage, a single-phase inverter structure can be designed to generate a reverse two-level voltage to the CMV. There are full-bridge structure and half-bridge structure in single inverters. In view of the cost, the simple half-bridge structure is the best choice. As shown in Fig. 4, the output voltage $v_{rcm}$ of the half-bridge is $\frac{kV_{dc}}{2}$. The counteractive voltage of the CMV can be generated. The class of the dc-side voltage in the active CM filter can be changed by the proportional coefficient $k$. This is useful for the flexibility in choosing switching devices.

There are two ways by which the active CM filter is coupled into the main circuit of the three-phase inverter. In the first way, the three-phase CM transformer with wideband is cascaded in the main circuit of inverter and the compensation of the CMV is in the form of voltage. Because of the drawbacks that are pointed out in Section I, this way is not considered in this design.

In the second way of compensating the CMV, the output current of the active circuit is injected into the main circuit through the filter network in parallel (as shown in Fig. 4). The essence of this method is to change the potential of the neutral point $n$ and to make it close to zero in theory.

According to Fig. 4, the CMV of the inverter’s output is

$$v_{cm} = \frac{(v_a + v_b + v_c)Z_{rcm} + v_{rcm}(Z_s + Z_p)}{(Z_s + Z_p) + 3Z_{rcm}}$$

Fig. 4. Structure of the active CM filter

$$v_{rcm} = \frac{v_{rcm}(v_a + v_b + v_c)}{(Z_s + Z_p)}.$$
This scheme can avoid the problem that the switching deadtime of three-phase inverters would have the negative impact on the control signal $S_{rcm}$. However, this scheme has two weak points. One is the delay from “detection” to “control.” The other is the active counteractive circuit has its own switching dead-time problem. To solve the former problem, a faster optocoupler can be adopted to detect the voltage and the signal process should be simplified as far as possible in the implementation. Thus the delay time of detection-control will be shortened. To solve the latter problem, the devices with short switching dead-time can be adopted. Considering the need of short switching dead-time devices and the fact that the switch frequency of the active counteractive circuit is the triple of the carrier frequency in the three-phase inverter, it will be a good plan to select power metallic oxide semiconductor field effect transistors (P-MOSFETs) and anti-parallel fast recovery diodes as the switches in the active circuit.

Under the conventional SPWM control, the THD of the output DMV in the three-phase inverter will be guaranteed to be less than the regulation limit through the design of $L/C_f$ filter. As analyzed in Section III, the THD of the output DMV in the three-phase inverter with CPPM is substandard markedly when the carrier frequency is low. Since most harmonic energy locates in the carrier frequency band filtering out the harmonics near the carrier frequency can greatly improve the DM characteristic of the inverter’s output.

What needs to be suppressed is mainly the carrier frequency harmonics, so a simple single tuned filter can be adopted to parallel in the line–line output of the three-phase inverter. There are two types of three-phase single tuned filters (see Fig. 6). In view of the connection with the active CM filter, the Y-type filter is better than the $\Delta$-type one. If the inductor $L_h$ and the capacitor $C_h$ in Fig. 6(b) are designed to satisfy

$$f_c = 1 / \left(2\pi \sqrt{L_h C_h}\right)$$

the single tuned filter can greatly suppress the harmonics near the carrier frequency. Because a capacitor $C_f$ in the original low-pass filter is in parallel with a branch circuit of the single tuned filter, they can be merged into the impedance $Z_p$ (as shown in Fig. 7). The passive DM filter is composed of the inductors $L_f$ in the original low-pass filter and the impedances $Z_p$.

**C. Hybrid Filter**

It will form an organic whole to connect the above designed active CM filter with the passive DM filter through the neutral point $n$. That is the hybrid filter in the design plan (see Fig. 7).
III. EXPERIMENTS

In the experiments, the switches of the inverter’s main circuit are implemented by insulated-gate bipolar transistors (IGBTs) and the switches of the active CM filter are implemented by P-MOSFETs. An induction motor, whose rated voltage is 380 V and rated power is 3 kW, is used as the load of the inverter. The other parameters of the experimental circuit (see Fig. 7) are listed in Table IV.

In the experiments, the detection-control scheme and the calculation-control scheme are implemented respectively in the processor as the control signals of the active filter’s switches. In Fig. 5, the reference sinusoids $v_{Aref}$, $v_{Bref}$, $v_{Cref}$, and the modulation index $M_a$ come from the closed-loop control unit of the inverter. Some transmission gates are inserted into the signal paths in Fig. 5. Its purpose is to compensate for the XOR gate or NOT gate on the other paths and to balance the delay times on the different driving paths. The strategy of the inverter is implemented in a field-programmable gate array (FPGA).

In the three-phase inverter with CPPM, the detection-control scheme and calculation-control scheme are adopted to drive the hybrid filter respectively. To ensure that the experiments are carried out under the same load conditions, the detection-control module [as shown in Fig. 5(a)] is still retained in the main circuit when the active CM filter is driven by the calculation-control scheme block [as shown in Fig. 5(b)]. A manual switch is used to switch the driving signals ($S_{rcm}$ and $S_{srcm}$) of the active CM filter between the output signals in Fig. 5(b) and the output signals of “Detection-control scheme” block in Fig. 5(a). The output CMV $v_{cm}$, CMC $i_{cm}$, and DMV $v_{AB}$ are measured under the above two schemes. In order to observe the influence of the CMV on the motor shaft, the shaft voltages $v_{shaft}$ of the motor are measured by a carbon brush. To compare with the above experimental results, $v_{cm}$ and $v_{AB}$ of the inverter without single tuned filter and active CM filter are also measured under the conventional SPWM strategy and the CPPM strategy, respectively.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Value</th>
<th>Commentary</th>
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<tbody>
<tr>
<td>$V_{dc}$</td>
<td>700 V</td>
<td>DC-side voltage</td>
</tr>
<tr>
<td>$L_f$</td>
<td>900 $\mu$H</td>
<td>Inductor of low-pass filter</td>
</tr>
<tr>
<td>$C_f$</td>
<td>25 $\mu$F</td>
<td>Capacitor of low-pass filter</td>
</tr>
<tr>
<td>$L_h$</td>
<td>90 $\mu$H</td>
<td>Inductor of single tuned filter</td>
</tr>
<tr>
<td>$C_h$</td>
<td>22 $\mu$F</td>
<td>Capacitor of single tuned filter</td>
</tr>
<tr>
<td>$R_h$</td>
<td>0.09 $\Omega$</td>
<td>Resistor of single tuned filter</td>
</tr>
<tr>
<td>$R_p$</td>
<td>1 M$\Omega$</td>
<td>Resistor for detecting CMV</td>
</tr>
<tr>
<td>$R_F$</td>
<td>230 $k\Omega$</td>
<td>Current-limiting resistor</td>
</tr>
<tr>
<td>$R_C$</td>
<td>4.7 $k\Omega$</td>
<td>Pull-up resistor</td>
</tr>
<tr>
<td>$L_{r1}$</td>
<td>300 $\mu$H</td>
<td>Inductor of active filter</td>
</tr>
<tr>
<td>$L_{r2}$</td>
<td>30 $\mu$H</td>
<td>Inductor of active filter</td>
</tr>
<tr>
<td>$C_{r1}$</td>
<td>75 $\mu$F</td>
<td>Capacitor of active filter</td>
</tr>
<tr>
<td>$C_{r2}$</td>
<td>66 $\mu$F</td>
<td>Capacitor of active filter</td>
</tr>
<tr>
<td>$R_r$</td>
<td>0.03 $\Omega$</td>
<td>Resistor of active filter</td>
</tr>
<tr>
<td>$f_0$</td>
<td>50 Hz</td>
<td>Output power-frequency</td>
</tr>
<tr>
<td>$f_c$</td>
<td>3.6 kHz</td>
<td>Carrier frequency</td>
</tr>
<tr>
<td>$t_{dead}$</td>
<td>5 $\mu$s</td>
<td>Switching dead-time of IGBT</td>
</tr>
<tr>
<td>$t_{dead1}$</td>
<td>1 $\mu$s</td>
<td>Switching dead-time of P-MOSFET</td>
</tr>
</tbody>
</table>

$L_{r1} = L_f/3, C_{r1} = 3C_f, L_{r2} = L_h/3, C_{r2} = 3C_h,$ and $R_r = |R_h/3$. The detailed parameters are listed in Table IV.
Fig. proposed matlab circuit

Fig. three phase inverter output
V. CONCLUSION

Through the above analysis and experiments, the hybrid filter, which is designed in this paper to suppress the CMV and DM harmonics of the three-phase inverter, is proved to have the following characteristics.

1) Simple in structure: Because it is ensured that the output CMV of the inverter can be two levels in any case by using the CPPM strategy, the simple half bridge is used in the hybrid filter to counteract the CMV. The simple structure means lower cost.

2) Easy in installation: As the added active DMV filter and single tuned filter in the hybrid filter are paralleled into the output lines of the inverter, they can be installed conveniently and are very suitable for the revamping of the established system.

3) Flexible in application: The proportional coefficient k provides the flexibility for the application design of the hybrid filter in various power levels.

4) Optimized in effect: As for the CMV suppression effect, the inverter with the hybrid filter is much better than that without the hybrid filter and the hybrid filter under the calculation-control scheme is superior to that under the detection-control scheme.

5) Compatible in THD standard: The phase-shifting of the carrier in the CPPM strategy enhances the output DM harmonics of the inverter in the carrier frequency band. Adding a single tuned filter in the hybrid filter suppresses the harmonics well and makes the output sinusoidal voltage meet the THD demand of loads.

REFERENCES


