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Design of DC Electronic Load

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***Abstract**: A DC electronic load plays a vital role in testing optimum operating characteristics of DC sources like batteries and power supplies. In this work a novel design topology is proposed which incorporates different testing mode together of a DC electronic load. The proposed regulated DC electronic load can operate in constant current, and power mode. The different operating modes are selected by the help of a push button processed by a microcontroller. Thereby different DC sources can be tested for instances batteries, power supplies, solar panels and hydrogen fuel cells. The results are presented at the end.*

***Keywords:** Electronic Load, operation of MOSFETs, Power MOSFETs.*

1. Introduction

Every DC source produced needs to be tested for its reliable operation, be it battery, power supplies (Switch Mode Power Supplies), solar panels or even hydrogen fuel cells. Different tests need to be performed on the DC sources in-order to determine the reliability of the source. For instance batteries need to be tested for discharge curves which gives us information's about battery discharge rates. Testing batteries aids in Estimating Battery Lifetimes. Similarly Power Supplies needs to be tested for full load conditions. Designers employ constant current mode for testing voltage sources and constant power mode for testing power range.

One way to load DC sources is to employ a high-power resistance network. When a high-power low resistance network is connected across the terminals of a battery, an estimated amount of current is sink by the load. In the resistive load the user won't have any control over the current absorbed by the resistive network as it is fixed resistor. Another performance issue with resistive network is that, as the battery is gets discharged, its voltage reduces leading to decrease in current sink by the resistors.

In order to overcome the limitations of resistive loads, electronic load are necessary. Many power electronic switches offer the ability to withstand high power dissipation with low internal resistance and high current handling capability. These features of power electronic switches are most suitable for electronic loads. Among various power electronic switches, the MOSFET (Metal Oxide Field Effect Transistor) offer low internal resistance, high power dissipation, high switching frequency and easy gate control. All these features make the MOSFET ideal for electronic load design. The earlier works on electronic load in limited to only constant current mode [1].

In this work, a DC electronic load was designed and fabricated with two different operating modes that is constant current mode and constant power mode. The topology mainly consists of a parallel power-MOSFET driven by an operational amplifier in voltage buffer configuration.

The detailed design procedure is addressed further.

2. Design

This unit deals with detailed design steps and selection of components.

2.1. Linear Mode of MOSFET

Power MOSFETs are widely used in power supplies and converters for their fast switching capabilities and reliable control. When a MOSFET is employed as a switch in a converter or a power supply the MOSFET is driven in the ohmic region. In order to utilize MOSFET for an electronic load it should be operated in the linear region. In the linear region we can have the control over the On-state resistance $R_{DS(on)}$. The typical output characteristics of a power MOSFET is shown in Figure 1. [3].

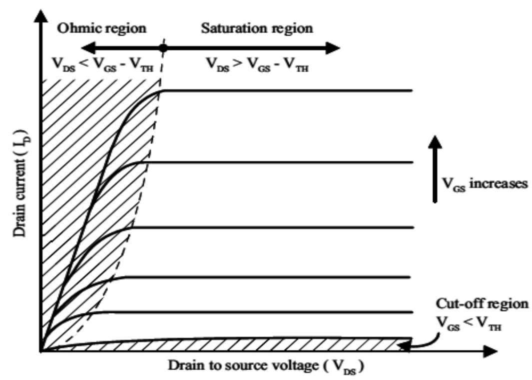

Figure 1. Characteristics of a power MOSFET [3].

2.2. Constant Current Operation

In order to sink the required amount of current, the load needs to offer very low resistance and capability to withstand high power dissipation. The MOSFET is made to work as a current drain in the current-regulation mode.

An operational amplifier can be employed to sense the current sink by the MOSFET and to regulate the gate voltage of the MOSFET by comparing with a reference set value [2]. The operational amplifier operates the MOSFET in linear region. A basic Constant current configuration is given in Figure 2.

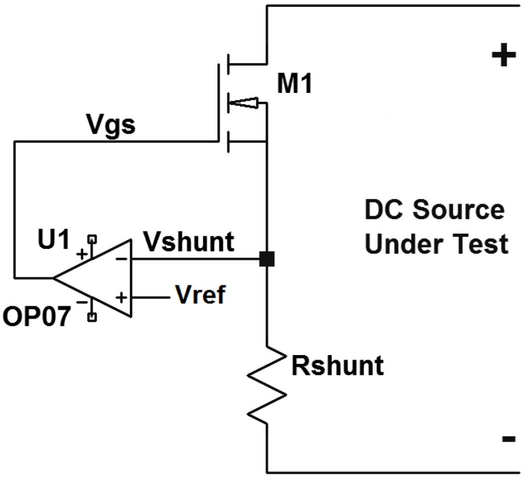

Figure 2. Current mode.

Here the non-inverting terminal of the operational amplifier should be given a reference voltage V_{ref} in accordance with the V_{shunt}. The reference voltage can be given by from a voltage divider or a rheostat. The MOSFET drain current I_D can be obtained from equation (1).

$$I_D = \frac{V_{GS}}{R_{shunt}} \quad (1)$$

The drain current I_D can be set as per the test requirements by adjusting MOSFET gate voltage, $V_{GS} = V_{ref}$. In the current mode a large amount of power is dissipated in the loaded MOSFET, care should be taken in order to operate the MOSFET under its rated Save Operating Area. It is feasible to parallel MOSFET in order to increase current handling capability and limit power dissipation per device.

Although MOSFET have a positive temperature co-efficient which makes them ideal for parallel operation, paralleling also increase the gate capacitance of the set-up making it prone to oscillations [4].

One way to make the parallel MOSFETs oscillations free is to include a resistor between the gate and the source terminals. This resistor R_{gs} prevents the charge build up in the gate capacitance and provides a safe passage for the charges to discharge. Another resistor R_g is added in the gate path in order to prevent clamping of the gate voltage when n number of MOSFETs are in parallel. The resistance R_{shunt} is the current shunt resistor. The inverting terminal of the operational amplifier receives the current I_D in the form of the voltage drop across the current shunt resistor that is V_{shunt}.

The shunt resistor further prevents unequal current distribution in the initial stages of operation of parallel MOSFETs [4]. The Figure 3 shows the placement of various resistors for optimum performance in parallel configuration.

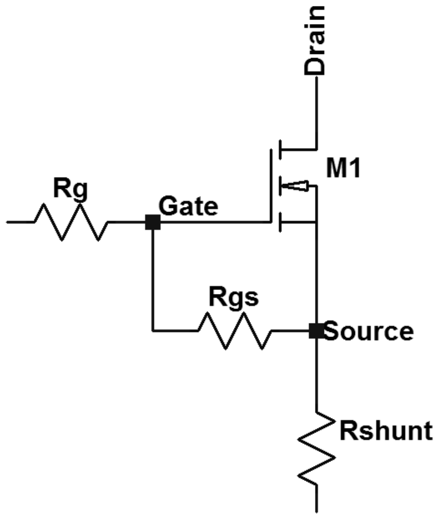

Figure 3. Equal current sharing requirements.

2.3. Constant Power operation

The constant power configuration, is similar to constant current mode. In this mode both the DC source voltage and the current is monitored and is maintained at the required constant power level.

A configuration can be built, so as to accommodate both constant current and power modes with the help of a push button switch and a microcontroller.

2.4. Gate Charge Q_g

The high power MOSFETs usually have a high gate charge Q_g. Also by paralleling n number of MOSFETs leads to a considerably high gate charge overall. This high gate charge expects a gate threshold voltage V_{GS} greater than the device threshold voltage V_{GSth} along with considerable current driving capability from the driver circuit.

In order to satisfy the high gate charge, a NPN BJT (Bi-Polar Junction Transistor) is employed in voltage configuration which can proved the required gate charge. The base terminal of the BJT is driven by the operational amplifier output. The design requirements based on the voltage, current are discussed.

2.5. Requirements

The design procedure is followed to accommodate the following requirements.

1) Maximum and Minimum Voltages: The DC source voltage under test has to be from 3V to 50V. Taking a convenient voltage range to test a Lead-Acid battery of rated 12V; 1Ah and a DC power supply of 18V; 1A rating.
2) Maximum Load Current: The maximum Load current for design is considered to be 5A maximum. The maximum current value determines the power dissipation in the load. Considering a low current reduces complexity.
3) Maximum Power: Although the product of maximum current and maximum voltage is 250W, the large power would require air-forced cooling. In order to reduce the size and cooling requirements a moderate 100W power as the maximum is considered.

2.6. The MOSFET

The MOSFET is the critical component. It should be able to withstand high power dissipation along with current carrying capability. Though specifically manufactured MOSFETs for linear operation are available, they are expensive. The Safe Operating Area of the MOSFET is essential in selection of a MOSFET. The Safe Operating Area IRFP250MPbF, is shown in Figure 4. In IRFP250, the drain current is

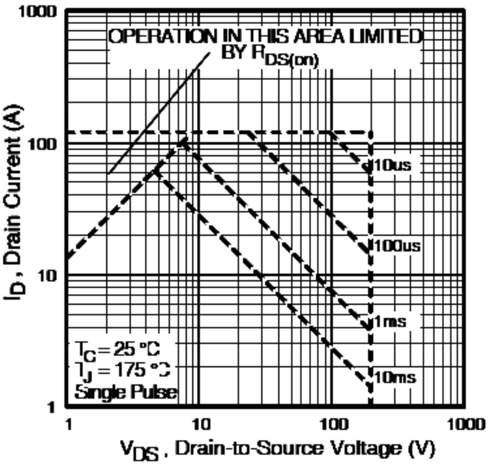

Figure 4. SOA of IRFP250 [6].

$I_D = 30A$, Power Dissipation is $P_D = 214W$, Static drain-to-source resistance *is* $R_{DS(on)} = 75m\Omega$ and drain to source breakdown voltage is $V_{DSS} = 200V$. It is in TO-247AC package which has better heat dissipation capability than TO-220 [6,7]. Considering the maximum voltage, current and power requirements all of them lie within the permissible limit in Figure 4. For the purpose of sinking 5A current a set of two branches of MOSFETs is opted.

2.7. Operational Amplifier

The role of operational amplifier in this application is essential. However there are no major specific requirements to meet by the operational amplifier. For the said application, the reliable industry op-amp LM358 is opted. If offers a drift of 7µV/°C, a non-zero offset in the order of mV, 0.7mA of supply current, with slew rate of 0.3Vµs which are preferable.

2.8. Shunt Resistor

The total current of the load will flow through the shunt resistance. Hence its selection is essential for the success of the design. The important factors to consider for selection are Power rating, and resistance value. The power dissipation in the resistor is maximum, hence a higher power rating resistor is essential which can be computed from equation (3).

$$P_{DRshunt} = \frac{{I_{LOAD}}^2 R_{Shunt}}{Number\ of\ parallel\ MOSFETs} \qquad (2)$$

From the equation (3) it is clear that a trade-off needs to reach in order to select shunt resistor in terms of cost, size and feasibility. It was decided to use a through hole Resistor of W21 Series of the following rating, $R_{shunt} = 0.33\Omega \pm 5\%$, $P_D = 3W$ and $V_{BD} = 100V$, Axial Leaded. The power rating and the voltage rating is twice the required by considering a safety factor of two.

The control signal for the operational amplifier is governed by equation (4) which is derived from the Ohm's Law.

$$\Delta V_{Control} = \frac{\Delta I_{LOAD} R_{Shunt}}{Number\ of\ parallel\ MOSFETs} \qquad (3)$$

From equation (4), it is computed that the control voltage range is found as 0 – 1.25mV for the specified drain current of 0 – 5A. This gives us the voltage to current ratio as 0.25mV /A.

2.9. Heat-sink Requirements

The thermal stability of the proposed design can only be confirmed if adequate cooling is provided. For the purpose of providing adequate cooling, an extruded aluminum heat sink is to be selected. The junction temperature can be calculated as [4,5]:

$$T_J = T_A + (R_{Tjc} + R_{Tcs} + R_{Tsa})P_{av} \qquad (4)$$

where T_A is the ambient temperature, R_{Tjc} is the junction-to-case thermal resistance, R_{Tcs} is the case-to-sink thermal resistance, R_{Tsa} is the sink-to-ambient thermal resistance, and P_{av} is the average power dissipation.

Considering the design specification of 100W maximum power. The data from device data sheet is

R_{Tjc} = *0.7°C/W,* R_{Tcs} = *0.24°C/W,* R_{Tsa} = *1.3°C/W* and T_A = *25°C,* i.e. room temperature, the junction temperature is found to be T_J = *100°C* for *50 W* power dissipation of each paralleled MOSFET. It is well below the specified maximum rating of *175°C* and can be tolerated by passive cooling offered by the heat-sink.

2.10. Proposed Set-up

The proposed set-up incorporating all the design challenges for efficient paralleling of MOSFETs, gate charge requirement, gate capacitance is presented here. The set-up also shows the various components involved.

In this set-up two power MOSFETs are in parallel configuration. The parallel combination of MOSFETS are driven by an operational amplifier. The setup is shown in Figure 5.

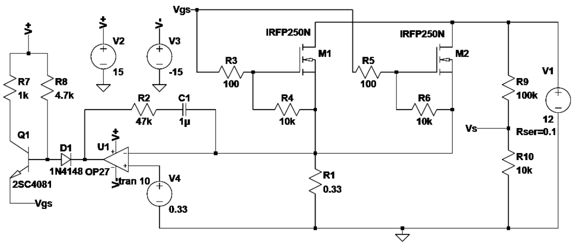

Figure 5. The electronic load set-up.

3. Fabrication and test

This chapter deals with the fabrication and test results. Following all the design steps, the circuit was build using two parallel blocks of MOSFETs. The positive terminal connection for the load is directly bolted on the heat-sink of the MOSFETs. A separate power supply of 12V is taken to energize the control circuit of operational amplifiers.

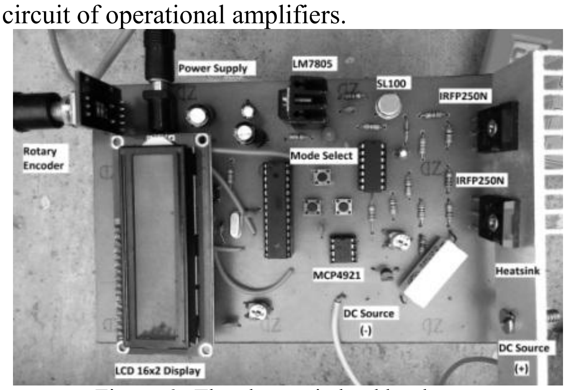

Figure 6. The electronic load hardware.

The A 12V, 1.2Ah rated lead-acid battery was tested the following results were obtained as shown in Figure 7.

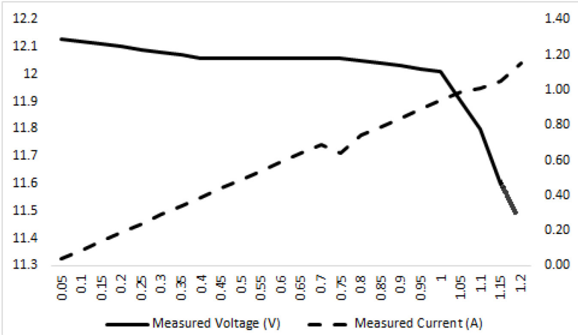

Figure 7. Testing of Lead-Acid battery.

4. Conclusion

The electronic loads are essential in the growing market of batteries and power supplies for testing purpose. In this work an attempt has been made to design a reliable and cost effective DC electronic load. From the above plot in Figure 7 we can conclude that the design for electronic load gives satisfactory results.

The future work that can be carried on the electronic load would be to include another operating mode that is constant resistance mode. The present set-up is not equipped to handle any fault conditions as of now, further work can be carried to include various protection features like over current, over voltage, reverse polarity, over temperature protection among others.

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