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Design and Implementation of Non-Volatile SRAM using Memristor

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Abstract*: There are many emerging and promising technologies which employs power-off mode to reduce the power dissipation of chips and to store the data even if the power supply is off. This Non-Volatility is achieved through many emerging Non-Volatile technologies like PCRAM, STTRAM, and Memristor etc. Memristive effect is more when we scale down our devices and its shows excellent operational characteristics in nanometer regime and it is the emerging promising technology having unique properties such as high density, good scalability and have low power. This paper provides a brief study of Memristor and proposes a Memristor based 6T SRAM cell. The Power on and off for the case of power failure is done here by the help of tri-state buffer and Memristor used in the circuit helps to restore the previously written bit thereby making the proposed SRAM Non-Volatile. .*

1. Introduction

As we know that from the very first days of electronics there are three fundamental circuit elements resister, capacitor, inductor and they are fully characterized. These three fundamental circuit elements defines five out of the six possible combinations of the fundamental circuit variables which are current, charge, voltage and the flux. In 1971 a paper was published by Chua and he theoretically presented the fourth circuit element named Memristor and defines the last possible combination. Memristor is the name derived from the combination of memory plus resistor. In his study Chua demonstrated that this memristance effect will be noticeable only in nanometer regime and thus this research remained dormant for the many decades.

In 2008 at Hewlett Packard (HP) labs a new wave of research was introduced in the field of circuit design as they successfully fabricated a Memristor. The Memristor fabricated was made up of thin film of doped and undoped Titanium dioxide sandwiched between two plates of platinium electrodes. Since then researchers are optimistic about it and its applications in the near future circuits which includes memory, sensors and artificial intelligence. Thus Memristor attracts lots of research interests because of its scalability, non-volatility, lower power consumption, and 3-D stacking capability [3]. These positive properties of Memristor in nanometer regime have resulted in applications in fields of non-volatile memory design [4], neuromorphic applications [5], programmable logic [6], analyzing non-linear circuits [7], digital and analog circuits [8]. Based on the study of Memristor and the devices formed by it. It is known that this can be scaled down to 10 nm or more and Memristor memories can achieve an integration density of 100 Gbits/cm which is few times higher than the advanced flash memory technologies that we use today.

2. Memristor

As we know that the conventional Nano scale CMOS technology are approaching their physical limits as oxide thickness is merely five layers of atom thus there is research going on the alternative technologies so that to meet the increasing computing and technology demands. If we move to the nanometer region then Memristor become crucial for future technology as memristance effect comes to play in nanometer region.

The Memristor is a device which is same like resistor but can change its intrinsic resistance depending upon the voltage applied across the two terminals. When there is no applied voltage or when the power supply is switch off then it remember its previous state and hold that resistance state. Thus making it perfect for non-volatile memory purpose. For the first time in 2008 Strukov linked this behavior to Chua's Memristor model. He claimed that a Memristor can be thought of as a thin semiconductor film having thickness D which is sandwiched between two contacts. There are two doped areas in the film, first is the doped area having width w and the other is the undoped area having width D-w. Thus we can say that the resistance of the doped and undoped region is the total resistance. By changing the width w we can change the resistance of the device. Figure 1 shows the physical model of the Memristor having doped and undoped region and figure 2 shows the circuit model having two series

resistances. By changing the width w the Ron and Roff are affected.

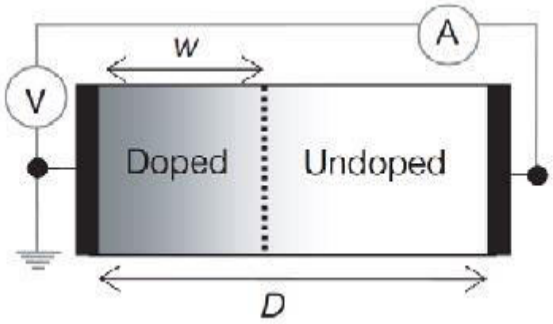

Figure 1.Memristor

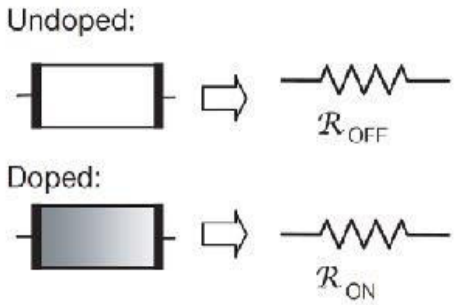

Figure 2.Resistance naming convention.

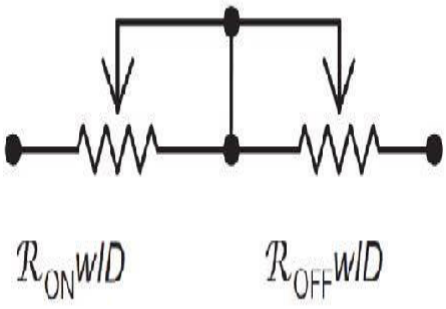

Figure 3.Effective electric structure of Memristor.

Mathematically it can be expressed as:

$$V(t) = \left(R_{ON}\frac{w(t)}{D} + R_{OFF}\left(1 - \frac{w(t)}{D}\right)\right) I(t) \quad (1)$$

Where V (t) is an external bias voltage which causes the charged dopants to drift, therefore adjusting w. The above equation is true for the simplest case of ohmic electronic conduction and the linear ionic drift in a uniform field having average ion mobility. The parameter w can then be expressed as:

$$w(t) = \mu_v \frac{R_{ON}}{D}\, q(t) \quad (2)$$

Thus from the above two equations we get:

$$M(q) = R_{OFF}\left(1 - \frac{\mu_v R_{ON}}{D^2}\, q(t)\right) \quad (3)$$

Where M(q) is the memristance.

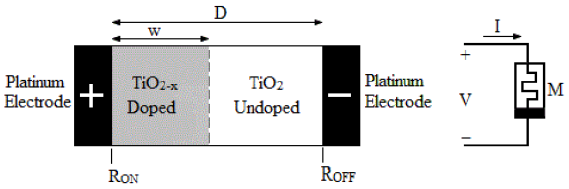

Figure 4.Circuit symbol of Memristor

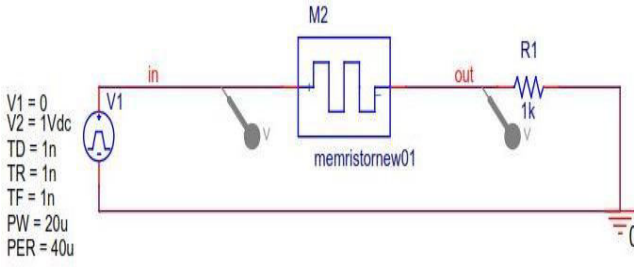

Figure 5.Applied input to Memristor.

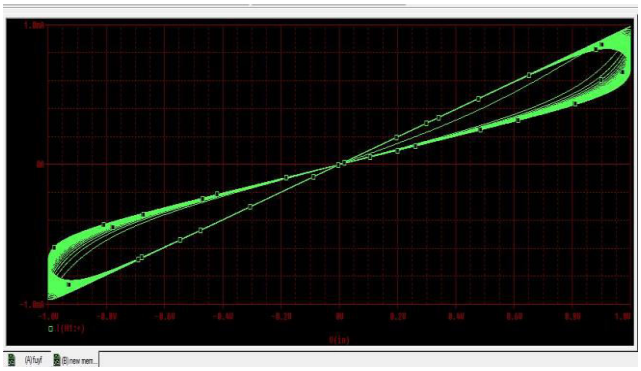

Figure 6.Characteristics of I-V curve.

Figure. 1 shows the device structure and Figure 4 shows the symbol of memristor used in electrical circuits. Figure 5 shows the applied square wave input and change in memristance of the memristor with the applied input voltage. I-V response of memristor to 1 V square wave is shown in Fig. 6. The I-V curve after simulation represents a pinched hysteresis curve, which is the memristor identification [1].

3. Conventional 6T SRAM Cell

This conventional 6T SRAM cell has poor stability and has low hold and read static noise margins. In the read operation, there is decrement in the cell scalability because of the voltage division between the access transistors and the driver transistor. The basic 6T SRAM cell consists of six MOS transistors. This SRAM cell provides less read

noise margin which further degrades due to process variation. To get high read noise margin in 6T SRAM cell the width of the pull down transistors has to be increased which further increases the problem of increase in leakage power dissipation. This 6T SRAM cell has more power dissipation and also has poor stability for small feature sizes at low voltage supply. During the storing operation, the stability of the cell decreases due to the voltage division between the access and driver transistors in the circuit.

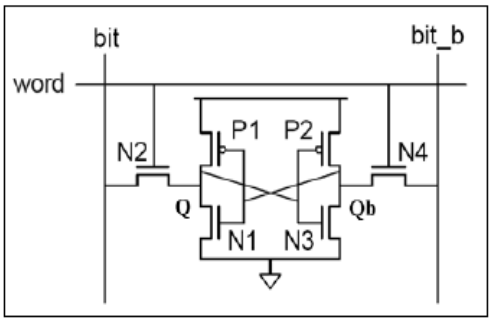

Figure 7.Conventional 6T SRAM Cell

4. Proposed Memristor based 6T SRAM Cell for Non-Volatility

The model for nonvolatile memory consist of 6T SRAM cell which has two back to back cross coupled inverters and has two access transistors. SRAM cell has three different states that are standby state, read state and write state.

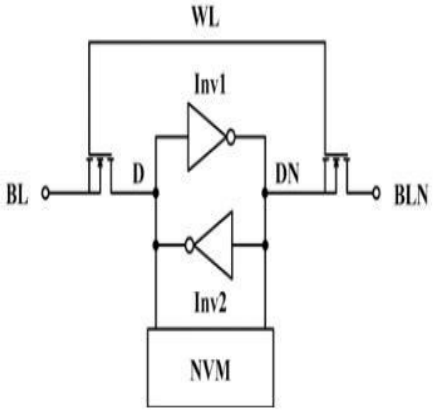

Figure 8. General models for NVM with 6T SRAM as a core

For the designing of SRAM cell the cell ratio and pull up ratio is the main thing which a designer have to concern about. If the cell ratio (CR) and pull up ratio (PR) are not defined properly then the chances that data will get destroyed is increased. Thus to conventional 6T SRAM cell the CR should be between 1-2.5 and the WR should be between 3-4. Cell ratio is the ratio of W/L of nmos transistor used in the cross coupled invertor and the access transistors. Whereas pull up ratio is the ratio of the pmos transistor and the access transistors.

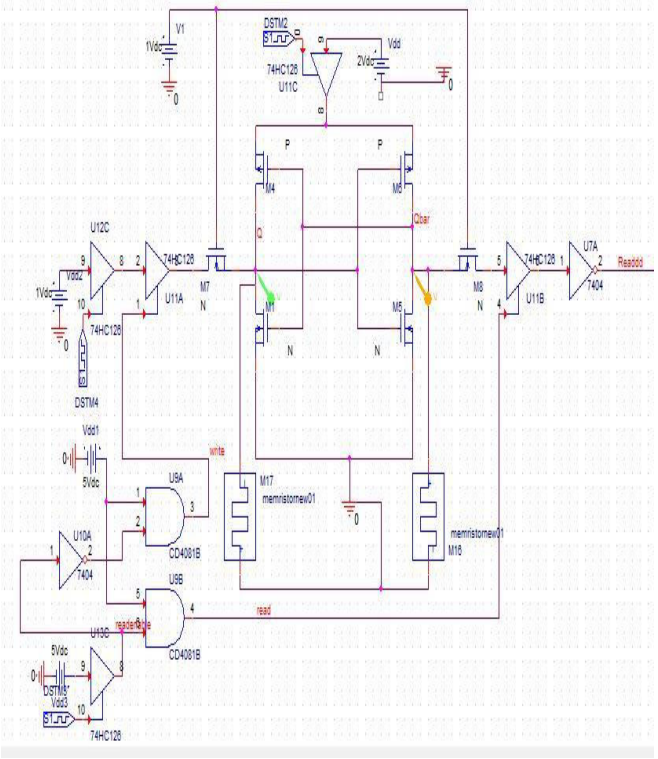

Figure 9. Proposed circuit of Memristor based SRAM

Here in this circuit two Memristor are connected each at the Q node and Qbar node. These are used to store the state which is written previously when the power supply is cut off. Here we use tri-state buffer which are used to pass the signal when the enable state signal is high (1). And if the enable signal is low (0), then no signal is transferred through the buffer. This property of buffer is used to cut off the power supply and thus when power supply is off memristor shows its behavior of holding the state. In the write process one of the Memristor goes in high impedance state and the other in low impedance state. The figure 10 shows the waveform of the Non-Volatile behavior of Memristor based SRAM.

WORKING: During the write 1 operation, logic 1 is to be written into the SRAM cell. For this to happen, CS is at high potential and WE is at low potential thus we get the write output from "and" gate as 1 which is the enable signal to the input buffer U11A to the bit line. Thus in write 1 case we have high potential at the bit line so all that high potential is passed through the buffer to the SRAM cell.
Thus accordingly on the functioning of SRAM cell Q gets high potential and Qbar gets low. Also at the

same time flux at Memristor M9 is higher than M10. Thus when power is switch off (here we use buffer to cutoff the power rails for a particular period of time), all the potential which is at Q and Qbar is grounded and also bitline is off. Thus when the power is supplied again then previous state at Q and Qbar is stored by the Memristors. This can be inferred from the read operation which is performed by setting CS to high potential and WE to high potential, this will enable buffer U11b and thus read operation is performed after that and we get 1 at the read output which demonstrate the working of the Memristor acting as a nonvolatile storage.

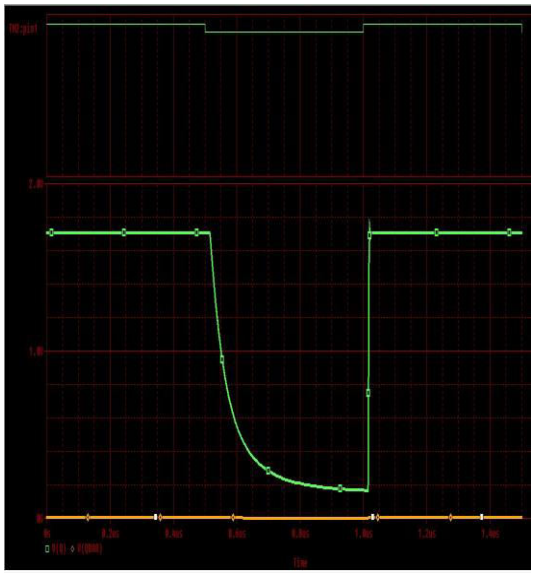

Figure 10.Waveform showing the Non-Volatile behavior

5. Results

This work focuses on design of non-volatile SRAM cell in the nanometer regime, where variations occur due to process and environmental parameters such as operating voltage, temperature, and noise. The power calculated after the simulation is shown below in table 1.

Table 1. Read and write dynamic power dissipation

Operation	Write 1	Write 0	Read 1	Read 0
Power dissipation(µw)	7.739	11.623	50.43	45.76

Table 2. Comparison between conventional and Memristor based SRAM cell

Operation	Proposed cell	Conventional cell
Power(mw)	0.127	10.373

6. Conclusion and Future Scope

Here in this paper we have proposed a CMOS-Memristor based SRAM cell and shows its Non-Volatility behavior. Also we have calculated the power dissipation and it comes low in comparison to the conventional 6T SRAM cell. Read and write time is little bit higher than the conventional 6T SRAM cell but can be improved with Memristor modeling and CMOS Fabrication technology.

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